TEGAM

Service and Operators Manual

TEGAM, INC.

SG5050
Programmable Leveled Sine Wave Generator

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

Please check for change information at the rear of this manual.

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Operator Safety Summary

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

Terms In This Manual

CAUTION — CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING — WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION — CAUTION indicates a hazard to property, including the equipment itself, and could cause minor personal injury.

WARNING — WARNING indicates solely a personal injury hazard not immediately accessible as you read the marking.

DANGER — DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols In This Manual

This symbol indicates where applicable cautionary or other information is to be found.

As Marked on Equipment

DANGER-High voltage.

Protective ground (earth) terminal.

ATTENTION-Refer to manual.

Power Source

This product is intended to operate in a power module connected to a power source that will not apply more than 250 volts RMS between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power module power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation. (I.E.C. Safety Class I)

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use The Proper Fuse

To avoid fire hazard, use only the fuse specified in the parts list for your product, and which is identical in type, voltage rating and current rating.

Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Do Not Operate Plug-In Unit Without Covers

To avoid personal injury, do not operate this product without covers or panels installed. Do not apply power to the plug-in via a plug-in extender.

Remove from Operation

If you have reason to believe that the instrument has suffered a component failure, do not operate the instrument until the cause of the failure has been determined and corrected.

Service Safety Summary

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing With Power On

Dangerous voltages may exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Use Care When Servicing With Covers Off

With the side and top covers off, access is available to several heatsinks and power resistors which can cause severe skin burns.

When operating the SG5050 outside the Power Module on flexible extender cables, a cooling fan should be used to blow air across the RF and Output Board heatsink. This is necessary to cool components for both service personnel safety and to prevent heat stressing electrical components.

Do Not Wear Jewelry

Remove jewelry prior to servicing. Rings, necklaces, and other metallic objects could come into contact with dangerous voltages and currents.

WARRANTY

Tegam warrants that this product will be free from defects in materials and workmanship for a period of one (1) year from the date of shipment. If any such product proves defective during this warranty period, Tegam, at its option, either will repair the defective product without charge for parts and labor, or will provide a replacement in exchange for the defective product.

In order to obtain service under this warranty, Customer must notify Tegam of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tegam, with shipping charges prepaid. Tegam shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tegam service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

This warranty shall not apply to any defect, failure or damage caused by improper use or improper or inadequate maintenance and care. Tegam shall not be obligated to furnish service under this warranty a) to repair damage resulting from attempts by personnel other than Tegam representatives to install, repair or service the product; b) to repair damage resulting from improper use or connection to incompatible equipment; or c) to service a product that has been modified or integrated with other products when the effect of such modification or integration increases the time or difficulty of servicing the product.

THIS WARRANTY IS GIVEN BY TEGAM WITH RESPECT TO THIS PRODUCT IN LIEU OF ANY OTHER WARRANTIES, EXPRESSED OR IMPLIED. TEGAM AND ITS VENDORS DISCLAIM ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. TEGAM'S RESPONSIBILITY TO REPAIR OR REPLACE DEFECTIVE PRODUCTS IS THE SOLE AND EXCLUSIVE REMEDY PROVIDED TO THE CUSTOMER FOR BREACH OF THIS WARRANTY. TEGAM AND ITS VENDORS WILL NOT BE LIABLE FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES IRRESPECTIVE OF WHETHER TEGAM OR THE VENDOR HAS ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

SECTION 1
SPECIFICATIONS

INTRODUCTION

This section of the manual contains a general description of the TEGAM SG 5050 Programmable Leveled Sine Wave Generator and its electrical, environmental, and physical specifications.

INSTRUMENT DESCRIPTION

The SG 5050 Programmable Leveled Sine Wave Generator is a GPIB programmable TM 5000-series plug-in instrument designed to provide a low-distortion sinusoidal waveform with leveled output amplitude. Frequency, amplitude and the front panel store/recall parameters are fully programmable. 8 seven-segment LEDs display parameter values in the display window. The SG 5050 output amplitude is programmable from 4.5mV to 5.5V peak-to-peak into 50Ω, and has a frequency range of 10KHz to 2500MHz with a programmable reference from 10KHz to 10MHz. Additional connectors provide timebase input and output reference signals to external sources.

At power-up, the instrument performs a self-test and assumes the settings in use when previously powered down, with the exception that the output is in the "OFF" condition. Up to twenty user-definable instrument configurations can be stored in memory.

Rear interface connections provide access to versions of all front panel signals except the main output.

Output Leveling Head

Each SG 5050 is provided with a matching Output Leveling Head. This leveling head must be installed on the SG 5050 at all times for proper operation.

A label attached to the leveling head cable identifies the serial number of the SG 5050 to which the leveling head is calibrated. If it is necessary to change leveling heads, the complete Adjustment Procedure must be performed to match the new leveling head to the SG 5050. After adjustment, it is recommended a new identification label be attached to the leveling head.

IEEE 488 (GPIB) Functions

The SG 5050 can be remotely programmed via the digital interface specified in IEEE Standard 488.1-1987, IEEE Standard Digital Interface for Programmable Instrumentation. In this manual, the digital interface is called the General Purpose Interface Bus (GPIB). The IEEE 488 factory address is set to 10.

The IEEE standard identifies the interface function repertoire of an instrument on the GPIB in terms of interface function subsets. The subsets that apply to the SG 5050 are listed in Table 1-1.

NOTE

Refer to IEEE Standard 488.1-1987 for more detailed information. The standard is published by the Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, New York 10017.

Table 1-1: Interface Function Subsets

Function	Subset	Capability
Source Handshake	SH1	Complete Capability
Acceptor Handshake	AH1	Complete Capability
Basic Talker	T6	Responds to serial poll. Untalks if My Listen Address (MLA) is received.
Basic Listener	L4	Unlistens if My Talk Address (MTA) is received.
Service Request	SR1	Complete Capability
Remote-Local	RL1	Complete Capability
Parallel Poll	PP0	Does not respond to Parallel Poll
Device Clear	DC1	Complete Capability
Device Trigger	DT0	Does not respond to GET
Controller Function	C0	No controller function
Electrical Interface	E2	Tri-state drivers

ELECTRICAL CHARACTERISTICS

Performance Conditions

The limits stated in the Performance Requirements column of the following tables are valid with the following conditions:

1. All measurements are made at the output connector of the Output Leveling Head. The SG 5050 must have been adjusted with the same leveling head that is used during specification verification measurements.

2. The SG 5050 internal adjustments are performed at an ambient temperature of +20°C to +30°C.

3. The SG 5050 must be in a noncondensing environment whose limits are described under Table 1-3, Environmental.

4. Allow thirty minutes warm-up time for operation to specified accuracy; sixty minutes after exposure to or storage in high-humidity or condensing environment.

Items listed in the Performance Requirements column of the Electrical Characteristics are verified by completing the Performance Check in the Service Manual. Items listed in the Supplemental Information and Description columns are provided for user information only and should not be interpreted to be Performance Check Requirements.

NOTE

The SG 5050 has been designed in accordance with the intent of UL Standard 1244, "Safety Requirements for Electrical and Electronic Measuring and Test Equipment."

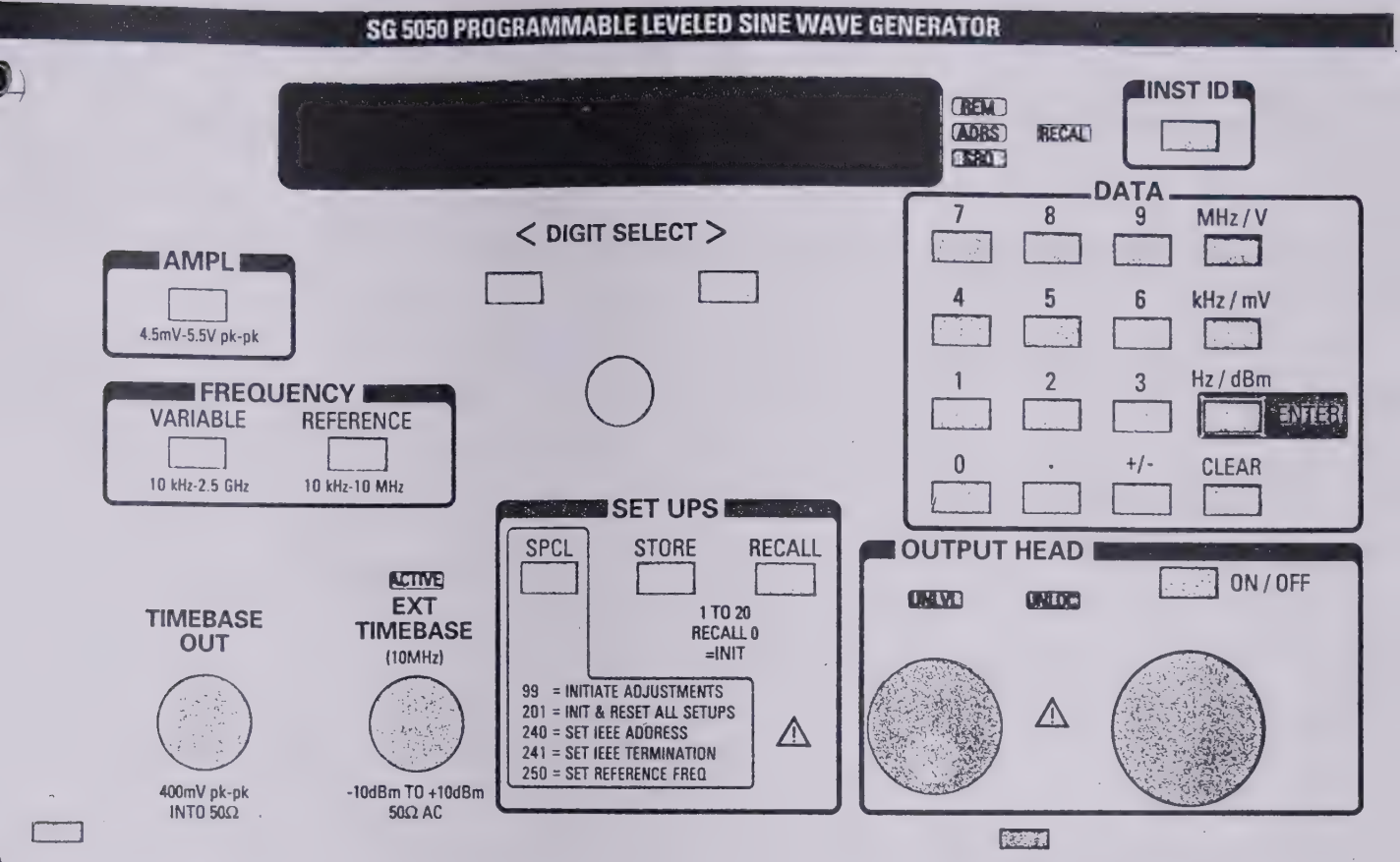


Table 1-2: Electrical

Characteristics	Performance Requirement	Supplemental Information
Frequency Range/Resolution		
10.000KHz to 49.999KHz		1Hz steps
50.00KHz to 550.00000MHz		10Hz steps
550.00000MHz to 1.500GHz		100Hz steps
1.500GHz to 2.500GHz		1000Hz steps
Frequency Accuracy		
Using Internal Timebase (within 1 year of last adjustment)		
10.000KHz to 49.999KHz	±(0.0003% of setting +0.3Hz)	
50.00KHz to 2.500GHz	±(0.0003% of setting +3Hz)	
Frequency Aging		1ppm/year
Using External Timebase (10MHz ±1.5ppm)		
10.000KHz to 49.999KHz		±(external timebase error +0.3Hz)
50.00KHz to 2.500GHz		±(external timebase error +3Hz)
Input Amplitude Requirement		-10dBm to +10dBm (70mV to 700mV RMS)
Input Resistance		50Ω AC, 500Ω DC
Lock Time		Less than 3 seconds

Electrical
(continued)

Characteristics	Performance Requirement	Supplemental Information
Timebase Out Output Frequency Frequency Accuracy Output Amplitude Output Resistance	 10MHz ±3ppm (using internal timebase)	 ±X ppm (using external timebase) Where X ppm is external timebase accuracy 400mV pk-to-pk into 50Ω 50Ω
Amplitude Range/Resolution 4.50mV to 55.00mV pk -to-pk 55.2mV to 550.0mV pk to pk 0.552 to 5.500V pk to pk -42.95dBm to +18.75dBm		 0.02mVolts peak to peak per step 0.2mVolts peak to peak per step 2mVolts peak to peak per step 0.05dBm per step
Amplitude Accuracy[1] (10KHz to 50KHz)	±1.5% of setting	
Amplitude Flatness 50.00KHz to 100MHz >100MHz to 250MHz >250MHz to 2.5GHz	 ±1.5% (of 50KHz ref) ±3% (of 50KHz ref) ±4% (of 50KHz ref)	Voltage peak-to-peak into 50 ohms
Output Source Resistance		50Ω, ±1%
Output DC Offset		<±1% of amplitude (Vpp) 20°C to 30°C <±2% of amplitude (Vpp) 0°C to 40°C
Output VSWR	Less than 1.2:1 up to 550MHz Less than 1.3:1 550MHz to 2.5GHz	

[1] Accuracy guaranteed only when the Leveling Head and SG 5050 have been calibrated together.

Electrical (continued)

Characteristics	Performance Requirement	Supplemental Information
Spectral Purity 10KHz to 49.999KHz		All harmonics and spurs less than –40dBc
50.00KHz to 1.1GHz at 5.5V Harmonics	Less than –30dBc 2nd harmonic typ Less than –35dBc 3rd harmonic typ Less than –40dBc all others	
1.1GHz to 2.5GHz at 3.33V	Less than –30dBc 2nd harmonic Less than –35dBc 3rd harmonic Less than –40dBc all others	
1.1GHz to 2.5GHz at 5.5V	Less than –25dBc 2nd harmonic typ Less than –30dBc 3rd harmonic typ	
Nonharmonics	Less than –40dBc	
Phase Noise	Less than –85dBc/Hz at 10KHz offset from 10KHz – 800MHz - 70dBc above 800MHz	
GPIB Setting Time Output OFF to ON All other function changes		From trailing edge of GPIB EOI until sine wave output is stable <150mS <80mS

Table 1-3: Environmental

Characteristics	Description
ESD	Meets IEC 802-2 ESD Test. Meets 20kV maximum discharge applied to instrument case per TEGAM Product Design
EMC[1]	Within conducted emissions limit for FCC Regulations, Part 15, Subpart J, Class A and Class B. Exceeds radiated emissions limit for FCC Regulations Part 15, Subpart J, Class A at the selected OUTPUT signal frequency.

[1] Tested with a TM5006A, Option 15 Power Module.

Table 1-4: Mechanical

Characteristics	Description
Maximum Overall Dimensions without leveling head	
Height	5.0"
Width	7.950"
Length	12.2"
Net Weight	
Standard Instrument including leveling head	7.0 lbs.

SECTION 2
OPERATING INSTRUCTIONS

INTRODUCTION

This section of the manual contains plug-in installation and removal instructions and describes the functions of the SG 5050 front panel controls, connectors and indicators. Operator's familiarization information is also provided as an aid in understanding how to operate the SG 5050 under local (manual) control.

Complete information for programming the SG 5050 via the GPIB (General Purpose Interface Bus) is found in the Programming section of this manual.

PREPARATION FOR USE

The SG 5050 is calibrated and ready for use when received. The SG 5050 is designed to operate only in the TM 5000-series power modules. Make certain the line selector block on the power module is positioned correctly.

The SG 5050 must also have the Output Leveling Head installed before use. The leveling head is calibrated to match the SG 5050. The two cables from the leveling head connect to the two OUTPUT HEAD connectors on the lower right portion of the SG 5050 front panel.

Installation and Removal

CAUTION

To prevent possible damage to the SG 5050, turn off the power module before installing or removing the instrument. Do not use excessive force to install or remove.

Check to see that the plastic barriers on the interconnecting jacks of the selected power module compartments match the cutouts in the SG 5050 rear interface connectors. If they do not match, do not install the SG 5050 until the reason is investigated. When the units are properly matched, align the SG 5050 chassis with the upper and lower guides of the selected compartments. Push the SG 5050 chassis in and press firmly to seat the rear-interface connectors in the interconnection jacks. Connect the two cables from the leveling head to the two connectors labeled OUTPUT HEAD on the SG 5050 front panel. Apply power to the SG 5050 by turning on the power module.

To remove the SG 5050 from the power module, ensure that the power is off, pull out both the release latches (located on the lower front panel) until the interconnecting jacks disengage and the SG 5050 slides out.

Repackaging For Shipment

If the instrument is to be shipped by commercial transportation, we recommend that it be packaged in the original manner. The carton and packaging material in which your instrument was shipped should be saved and used for this purpose.

If the original package is unfit for use or not available, package the instrument as follows:

1. Obtain a corrugated cardboard shipping carton with 200-pound test strength and having inside dimensions at least six inches greater than the instrument dimensions.

2. Wrap the instrument with polyethylene sheeting or equivalent material to protect the finish.

3. Cushion the instrument on all sides by tightly packing dunnage or urethane foam between the carton and the instrument, allowing three inches on each side.

4. Seal the carton with shipping tape or with an industrial stapler.

FRONT PANEL CONTROLS, CONNECTORS AND DISPLAY

All controls necessary for local operation of the SG 5050 are located on the instrument front panel. Some push buttons illuminate to provide visual indication that associated functions are active. A brief description of these controls, connectors and indicators follows. Refer to Figure 2-1.

1 DISPLAY INDICATORS

The SG 5050 uses seven-segment LEDs to display a numerical value up to eight digits. In addition, LED indicators in the left and right areas of the display window illuminate when appropriate to indicate the selected function modes and parameter units of measure.

Function Mode

The illuminated mode indicator in the left side of the readout display window defines the function. The two function modes are:

AMPL Activated when the AMPL button is pressed.

FREQ Activated when the FREQUENCY VARIABLE or REFERENCE buttons are pressed.

Parameter Units of Measure

The illuminated units indicator in the right side of the readout display window defines display value units. These units are:

MHz Activated when the FREQUENCY VARIABLE button is selected. Frequency selected is from 1MHz to 2500MHz.

KHz Activated when the FREQUENCY VARIABLE button is selected. Frequency selected is from 10.0KHz to 999.99KHz.

V Activated when the AMPL button is selected. Amplitude selected is from 1V to 5.500V.

mV Activated when the AMPL button is selected. Amplitude selected is from 4.5mV to 998mV.

dBm Activated when the AMPL button is selected. Amplitude selected is from –42.95dBm to +18.75dBm.

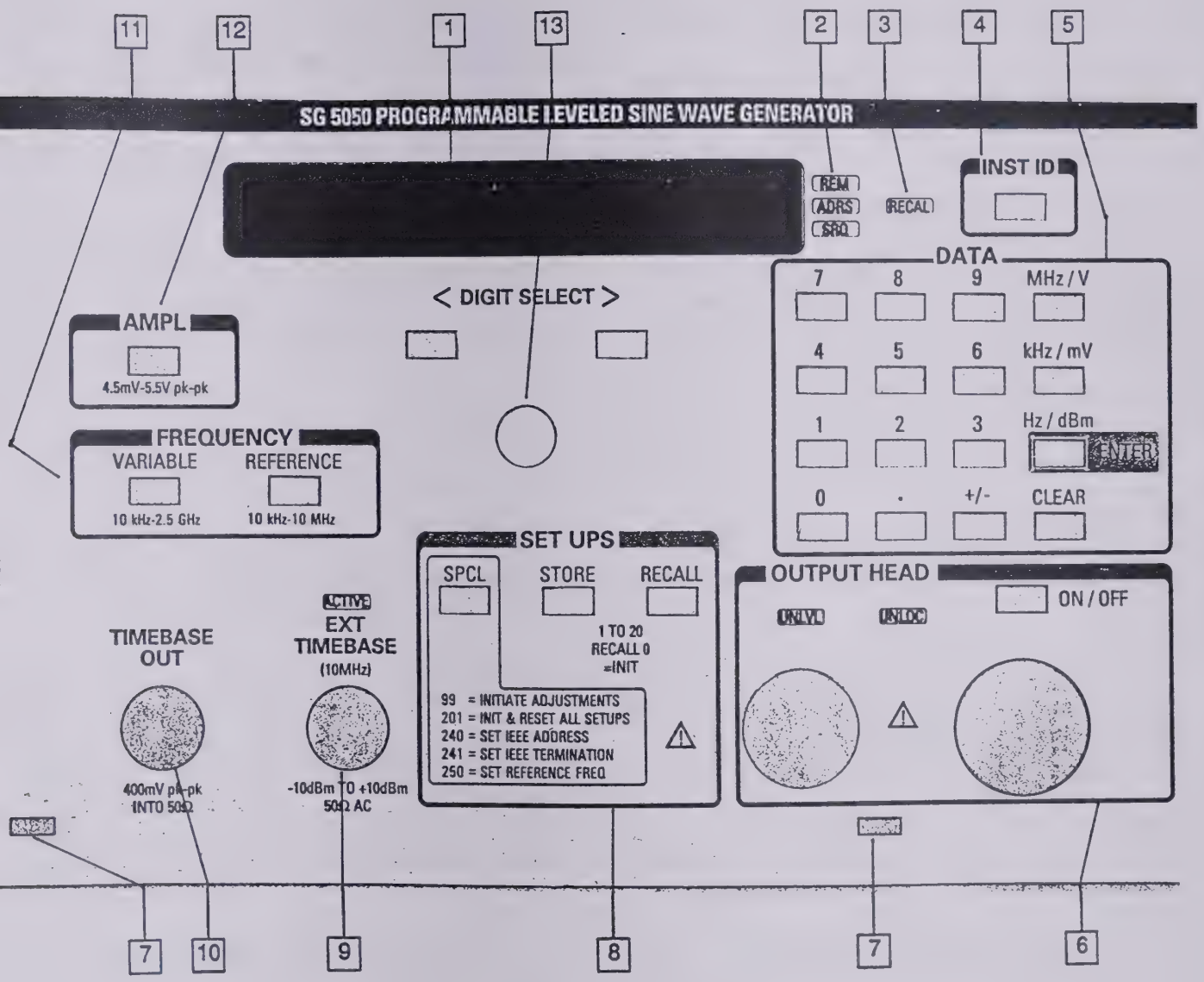


FIGURE 2-1: Front Panel Controls and Connectors

2 GPIB STATUS INDICATORS

The current status of the GPIB is shown by the illuminated indicators just to the right of the readout display window. They are:

REM Illuminates when the SG 5050 is operating under remote control via the GPIB.

ADRS Illuminates when the SG 5050 is addressed via the GPIB.

SRQ Illuminates when the SG 5050 has detected an error or event. The controller must conduct a serial poll to query the error or event and to extinguish the SRQ indicator.

NOTE

At power-on the SRQ indicator is illuminated. This may not indicate an error condition but only that the power-on SRQ has occurred and has not yet been serviced by a GPIB controller.

3 RECAL INDICATOR

Indicates the loss of the calibration constants. Most likely this is due to nonvolatile memory failure. This indicator will remain illuminated until the instrument has been readjusted by performing the Adjustment Procedure in the Service Manual.

4 INST ID PUSH BUTTON

Causes the SG 5050 to display its primary GPIB address and message terminator. If USEREQ has been enabled, it will generate a Service Request (SRQ) over the GPIB.

The message terminator currently selected in the SG 5050 (either EOI or LFEOI) will be displayed in the readout display window.

See Section 3 Programming for instructions to change the GPIB address and to select the message terminator required by your controller.

5 DATA ENTRY KEYPAD

0 through 9, Decimal point, +/-

Used to enter a numeric value for the amplitude, frequency or the argument when using STORE, RECALL or SPCL.

MHz/V, KHz/mV, Hz/dBm

Used to terminate the entry of a parameter value and specify the unit of measure after you have selected the amplitude or frequency function. The appropriate unit will illuminate in the readout display window, indicating the selected unit.

ENTER

Used only with the front panel SET UPS, entry of the STORE/RECALL storage locations, and the SPCL push button functions (e.g., setting the GPIB address).

CLEAR

Used to delete a partial entry. The SG 5050 will return to the previous valid instrument settings.

Also used after STORE or RECALL is pressed to cancel the STORE or RECALL operation and reset the display.

6 OUTPUT LEVELING HEAD

Connectors

The Output Leveling Head provides the connection between the SG 5050 and the Instrument-Under-Test. Within the leveling head are attenuators, signal level sense detectors and precision impedance matching circuits. The leveling head must be used for all SG 5050 operations and should be connected directly to the

load to maximize performance. The use of extension cables, matching networks, transformers, etc., between the leveling head and the Instrument-Under-Test can cause performance degradation due to transmission losses and reflections.

If extension cabling is absolutely necessary between the leveling head and the Instrument-Under-Test, coaxial air line is recommended to minimize frequency dependent losses that affect the apparent leveling performance.

Two cables connect the leveling head to the SG 5050. The N connector cable carries the output signal, and the multiwire cable carries control and status signals back to the SG 5050. If the multiwire cable is disconnected, the SG 5050 output will be automatically turned off. If only the N cable is disconnected, the SG 5050 signal may still be present at the front panel N but it is effectively removed from the Instrument-Under-Test.

The SG 5050 is adjusted and shipped from the factory with a matching leveling head. The serial number on the leveling head cable must match the SG 5050 serial number for calibrated operation. Do not interchange leveling heads between instruments, as performance may no longer be to specification. If the leveling head is interchanged, the complete calibration Adjustment Procedure must be performed before use.

ON/OFF Push Button

Disconnects the sine wave signal output from the leveling head. The output impedance at the signal output connector remains at 50Ω.

UNLVL Indicator

When illuminated, indicates sine wave output is unleveled (e.g., excessive loading, open signal or control line, leveling circuit failure, etc.).

UNLOC Indicator

When illuminated, indicates one of the frequency setting loops is not locked to the timebase reference frequency (e.g., out-of-range reference signal, circuit failure, etc.).

7 RELEASE LATCHES

Plug-in release latches. Pull both latches to remove the SG 5050 from the power module.

8 SET UPS

STORE Push Button

Stores the current instrument setting in the specified user-definable storage location. Twenty locations (1 through 20) are available. Instrument settings are retained in memory when the instrument is powered down.

RECALL Push Button

Recalls an instrument setting from user-specified storage locations (1 through 20) and configures the instrument to those settings. Recall 0 configures the instrument to factory-default settings that are the same as the INIT settings.

SPCL Push Button

- Allows you to initialize the current front panel settings and all twenty storage location setups at one time.
- Used in the Adjustment procedure to change calibration constants.
- Allows you to set the GPIB address or message terminator from the front panel. See Section 3 Programming.
- Allows you to set the reference frequency.

9 EXT TIMEBASE CONNECTOR

Allows the SG 5050 timebase to be frequency-locked to a precision external 10MHz reference frequency.

ACTIVE Indicator

Indicates the external 10MHz reference frequency signal has sufficient amplitude and approximately the correct frequency to lock the internal timebase.

10 TIMEBASE OUT CONNECTOR

Provides the internal 10MHz timebase frequency output to frequency lock other signal sources to the SG 5050.

11 FREQUENCY

VARIABLE Push Button

Selects the variable frequency function. Allows you to vary the sine wave output frequency, using the control knob or the DATA keypad. Frequency values can be selected in hertz, kilohertz or megahertz.

The VARIABLE push button and the FREQ indicator in the readout display window are both illuminated when the VARIABLE function is active.

REFERENCE Push Button

Selects the variable reference frequency, and displays the reference frequency in the readout display window. To return to the variable frequency setting that was last selected, press the VARIABLE push button.

The REFERENCE push button and the FREQ indicator in the readout display window are both illuminated when the REFERENCE function is active.

12 AMPL PUSH BUTTON

Selects the variable amplitude function. Allows you to vary the sine wave output amplitude using either the control knob or the DATA keypad. Amplitude values can be selected in volts, millivolts or dBm.

The AMPL indicator in the readout display window and the AMPL button is illuminated when the amplitude function is active.

The amplitude can be set in either the REFERENCE or VARIABLE FREQUENCY mode and remains the same when switching between modes.

13 CONTROL KNOB

Varies the value of the selected parameter. The smallest rate of change (increment) of a digit is determined by the mode and range that you select. For example, if you are in the amplitude mode and have selected a value within the range of 0.552V to 5.500V, the readout will increment or decrement in as small as 2mV steps.

DIGIT SELECT Push Buttons

Selects the control knob resolution (i.e., the digit that will change when the control knob is rotated).

Each push of the left or right button will cause the selected digit to blink as it steps one place left or right.

On the rear panel of the SG 5050 is a four position DIP switch that is used to configure the instrument at power-up. These switches are used to activate service functions and will not need to be used under normal operation. Their function, however, is described briefly below.

For normal operation, all toggles are set for open contacts (the contacts are closed when the toggle is depressed to the left, facing the rear of the instrument).

The following functions are activated when the contacts are closed:

Toggle	Function
1	Reinitialize firmware
2	Diagnostic bypass
3	Enable adjustment
4	Not used

OPERATOR FAMILIARIZATION

General Operating Information

With the SG 5050 properly installed in the power module, allow 20 minutes warm-up time for operation to specified accuracy; 60 minutes after storage in or exposure to a high humidity (condensing) environment.

Power-Up Sequence

When powered up, the SG 5050 performs a diagnostic self-test to check the functionality of its ROM, RAM and some hardware circuits. It also illuminates all front panel LEDs and indicators. If a self-test error is detected, and E followed by a three-digit error code will appear in the readout window indicating an internal malfunction. Should this occur, refer the condition to qualified service personnel. Pressing any button clears the error code from the readout window and allows the instrument to complete initialization, but does not clear the condition causing the error code. If more than one error has been detected, a button may have to be pushed several times to clear each of the errors in turn from the display.

Upon successful completion of the self-tests, the SG 5050 restores the instrument settings that were in use when the instrument was last turned off. The sine wave signal to the output head, however, will always be turned off at power-up.

In addition, the SG 5050 always powers up with the frequency displayed in the display window and with the control knob digit select resolution set to the default value.

Initializing the Instrument Settings

You can initialize the current front panel settings, or all twenty of the instrument setting storage locations at one time.

To initialize the current front panel settings:

1. Press the RECALL button.
2. Enter 0 (zero) on the DATA keypad.
3. Press the ENTER button.

The SG 5050 is now initialized to the following settings.

Output ON/OFF	OFF
AMPL	1.000V
FREQUENCY	10.00000MHz
Reference (50KHz)	OFF
Variable (10KHz-2500MHz)	ON
RQS	ON
USEREQ	OFF
SREFREQ	50.00KHz

To initialize the current instrument setting and all twenty of the storage locations:

1. Press the SPCL button.
2. Enter 201 on the DATA keypad.
3. Press the ENTER button.

The instrument settings and all storage locations are now initialized to the settings listed above.

Function and Parameter Selection

The SG 5050 generates an amplitude-leveled sine wave signal with two variable functions, amplitude and frequency. The parameters of these two functions are set from the front panel using either the control knob or the DATA entry keypad (for GPIB operation, refer to Section 3

Programming). The ranges for each function and the parameter resolutions are specified in Section 1 Specification of this manual.

Setting Amplitude Parameters

To select a specific amplitude value, press the AMPL button. The amplitude parameter and unit of measure last selected will appear in the readout display window.

Voltage Resolution vs. Range

Voltage Range	Resolution
-42.96dBm to +18.75dBm	0.05dBm
4.50mV to 55.00mV	0.02mV
55.2mV to 550mV	0.2mV
0.552V to 5.500V	2mV

Next, enter the desired amplitude value using either the control knob or DATA entry keypad as follows:

Control Knob Entry

Press the DIGIT SELECT buttons to select the significant digit you wish to change (each digit will blink once when selected). Clockwise knob rotation will increment the selected digit, and counterclockwise rotation will decrement the selected digit.

DATA Keypad Entry

Select the numeric value first and then the units desired (e.g., V, mV or dBm) on the keypad; this action enters the selected amplitude value. If the amplitude value entered on the keypad has a higher resolution than is allowed the SG 5050 will round it off to the nearest allowable setting.

Setting Frequency Parameters

To select a specific frequency, press the VARIABLE FREQUENCY button. The frequency parameter and unit of measure last selected will appear in the readout display window.

Frequency Resolution vs. Range

Frequency Range	Resolution
10.000KHz to 49.999KHz	1Hz
50KHz to 550.0000MHz	10Hz
550.0000MHz to 1.500GHz	100Hz
1.500GHz to 2.500GHz	1000Hz

Next, enter the desired frequency value using either the control knob or DATA keypad as follows:

Control Knob Entry

Press the DIGIT SELECT buttons to select the significant digit you wish to change (each digit will blink once when selected). Clockwise knob rotation will increment the selected digit, and counterclockwise knob rotation will decrement the selected digit.

DATA Keypad Entry

Select the numeric value first and then the units desired (e.g., Hz, KHz or MHz) on the keypad; this action enters the selected frequency value. If the frequency value entered on the keypad has a higher resolution than is allowed, the SG 5050 will round it off to the nearest allowable setting.

Table 2-1: Front Panel Error Codes

Error	Description
250	Not in adjustment mode
350	Unleveled
354	VCO Board PLL unlocked
355	DDS PLL unlocked
356	Unplugged
357	Head temperature error/leveling A/D error
363	Battery RAM error, store settings lost
364	EEPROM error, cal constants lost
365	CPU to DDS communication error
GPIB Only Errors	
103	Value not valid
151	Error in command or syntax error
205	Error in number, value out of range or a bad symbol
401	Power on event
403	ID/User request
455	SRQ pending

Setting the Reference Frequency

Press the REFERENCE FREQUENCY button. The readout window will display the reference frequency value. You can set the reference frequency amplitude by selecting the AMPL button and entering the desired amplitude as described under Setting Amplitude Parameters above.

Select the VARIABLE FREQUENCY button to return to the previous variable frequency settings and to turn off the reference frequency. The amplitude will be the same as the reference frequency amplitude.

Changing the Programmable Reference Frequency

The SG 5050 has a programmable reference frequency. To change the reference frequency, press the SPCL key, the digits 250, followed by the ENTER key. The SG 5050 will then display the current value of the reference frequency. Use the keypad to enter the new value, and press the KHz or MHz keys to enter the new value. If the frequency value entered on the keypad has a higher resolution than is allowed, the SG 5050 will round it off to the nearest allowable setting. The range is 10KHz to 10MHz.

Storing and Recalling Instrument Setups

You can store up to 20 instrument setups in a battery backed-up nonvolatile RAM. To store a setup, set the instrument parameters and units of measure as desired, and press the STORE button. Enter a storage location between 1 and 20 on the DATA keypad, and press the ENTER button. The current instrument setup is now stored in that location (in nonvolatile RAM) and will be retained when the instrument is powered down.

To recall a specific set of instrument settings, first press the RECALL button, enter any previously set storage location (1 through 20) on the DATA keypad, then press the ENTER button.

Displayed Errors

When powered up, the SG 5050 performs a diagnostic self-test to check its functionality. If an error is found, an error code will be displayed in the display window. Pressing any key can clear the error. Error code definitions are listed in Table 2-1.

If no error is found during self-test, the SG 5050 restores the instrument settings that were in use when the instrument was last turned off, except the output is OFF.

Special Functions

The SG 5050 has several special functions that allow the user to check or change operational settings. These functions are listed in Table 2-2.

To invoke an SPCL function, press the SPCL button. Then enter the two or three digit SPCL code and press ENTER.

Output Loading

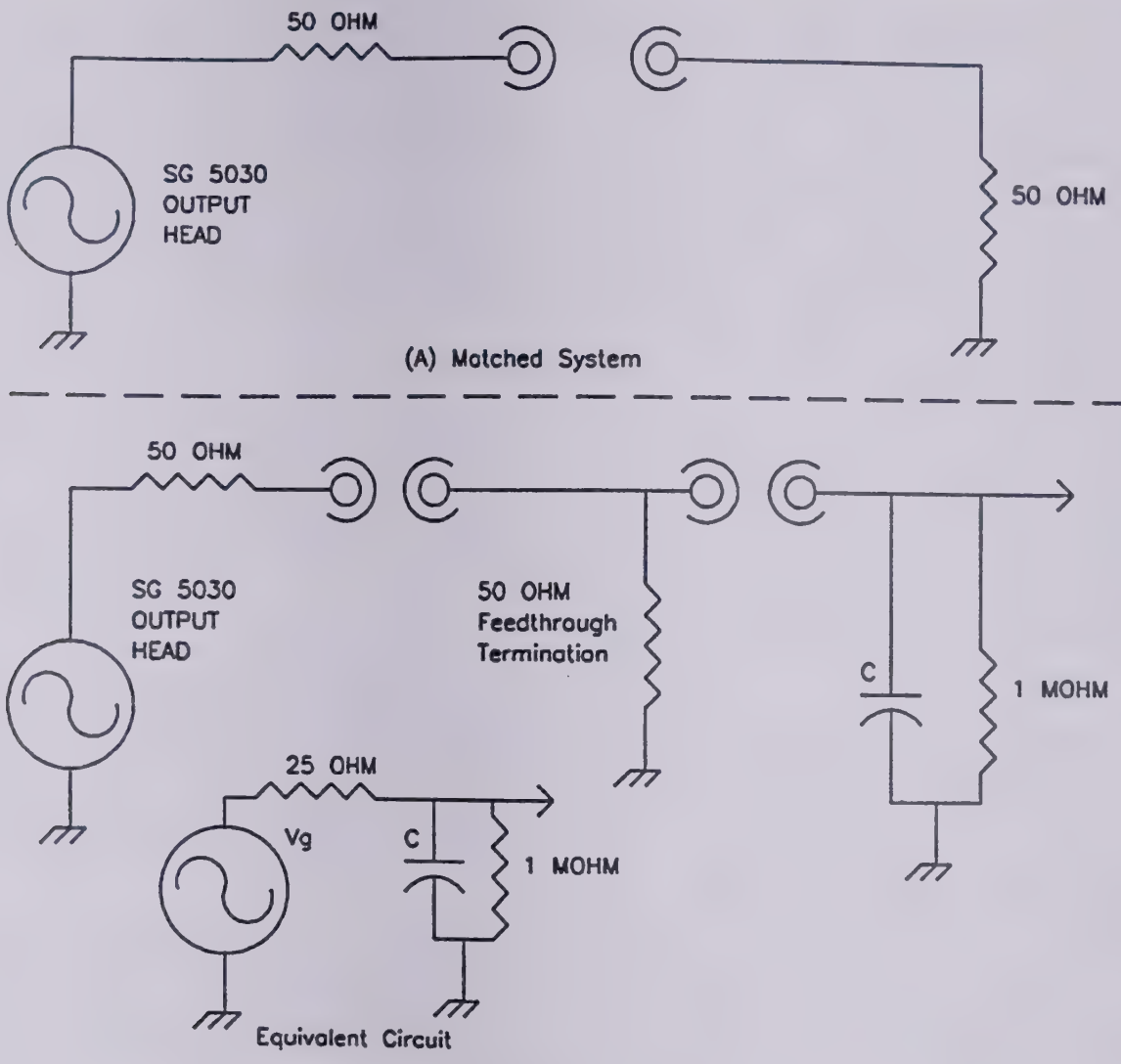
The SG 5050 is designed to operate into a 50Ω impedance load at the leveling head output connector. If load impedance is substantially greater than 50Ω, connect a low-loss precision feed-through termination of the appropriate value to the leveling head, and then make connection to the load. Refer to Figure 2-2(B) for reference.

NOTE

When lit, the UNLVL light on the front panel indicates a mismatched load or that the output is shorted. When the leveling head is disconnected from the front panel, the UNLVL light is also illuminated, and the instrument will turn its output off.

Table 2-2: Special Functions

Code	Description
99	This function initiates the instrument calibration process and is intended for use by qualified service personnel only. If the user accidentally selects this function, the instrument will show error code E250 (not in adjustment mode) in the display window, indicating the internal DIP switch toggles have not been set to allow adjustment.
201	Initializes the current front panel settings and all twenty storage location setups at one time. See Initializing the Instrument Settings earlier in this section.
240	Shows the current GPIB address in the display window, and allows the user to enter a new address from the keypad, if desired. See Resetting the GPIB Address and Message Terminator in Section 3 Programming.
241	Shows the currently selected message terminator in the display window, and allows the user to select either LFEOI or EOI. See Resetting the GPIB Address and Message Terminator in Section 3 Programming.
250	Allows the reference frequency to be set.



Generator frequency is F and F_{co} is $1/(2\pi RC)$, the 3dB cutoff frequency. When the output head is terminated with a 50Ω feedthrough terminator, the value of R is 25Ω.

FIGURE 2-2: Signal Termination Configurations

The SG 5050 adjusts signal amplitude and distortion at the leveling head. To maintain signal integrity, it is important to minimize adapter and transmission line discontinuities and reflections between the leveling head and the Instrument-Under-Test. Adding coaxial cable or other devices between the output head and the load impairs the constant amplitude function, since transmission line insertion losses vary with frequency.

If there is a DC voltage across the load, use a DC blocking capacitor between the output head and the load. A DC blocking capacitor, listed in the Optional Accessories list in the Service Manual, can be used with minimal loss at frequencies greater than 1MHz.

A DC block is also useful as a protective device when the SG 5050 signal is applied to RF equipment that is sensitive to DC voltage, such as some spectrum analyzer inputs. Although the SG 5050 has no DC offset, it can output high amplitude low frequency AC signals that might be a problem to some sensitive RF circuits.

If signal amplitudes less than the minimum (4.5mV p-p) are desired, use appropriate attenuators connected between the leveling head and the device under test.

NOTE

TEGAM BNC attenuators with –02 suffix are recommended. Other attenuators may be used, however, measurement accuracy might be compromised.

When operating the SG 5050, always consider the total load impedance and its effect on the output amplitude. The input capacitance of the equipment under test will affect the bandwidth. The equivalent circuit shown in Figure 2-2 is useful in estimating the amplitude changes caused by capacitive loads. Note that as system input capacitance increases, output signal decreases.

MAKING BANDPASS MEASUREMENTS

Making bandpass measurements are easy with the SG 5050. Basically, a reference amplitude at the device-under-test output is set at a reference frequency, then the SG 5050 frequency is increased (or decreased) until the device-under-test output decreases by 3dB (29.3%) from the reference amplitude. This is shown graphically in Figure 2-3. It is important that the reference amplitude be set at a frequency where the device-under-test is known to be linear. For most devices, the 50KHz reference frequency of the SG 5050 is valid, though other frequencies may be used. An oscilloscope whose bandwidth is substantially greater than the device-under-test makes an ideal measurement device for bandwidth checks.

1. Connect the oscilloscope to the output of the Device-Under-Test (DUT). To make the bandwidth measurement, set the reference frequency amplitude first. Adjust the SG 5050 output amplitude, the DUT gain and the oscilloscope controls to display a sine wave of exactly six divisions, as shown in Figure 2-4.
2. Next, slowly increase (or decrease) the SG 5050 frequency until the oscilloscope display is reduced to 4.2 divisions, as shown in Figure 2-5. Allowing the oscilloscope trigger to free-run might make the display amplitude easier to judge. Do not adjust the gain or amplitude controls during this step.
3. Check the SG 5050 frequency readout display. This is the –3dB frequency of the DUT.

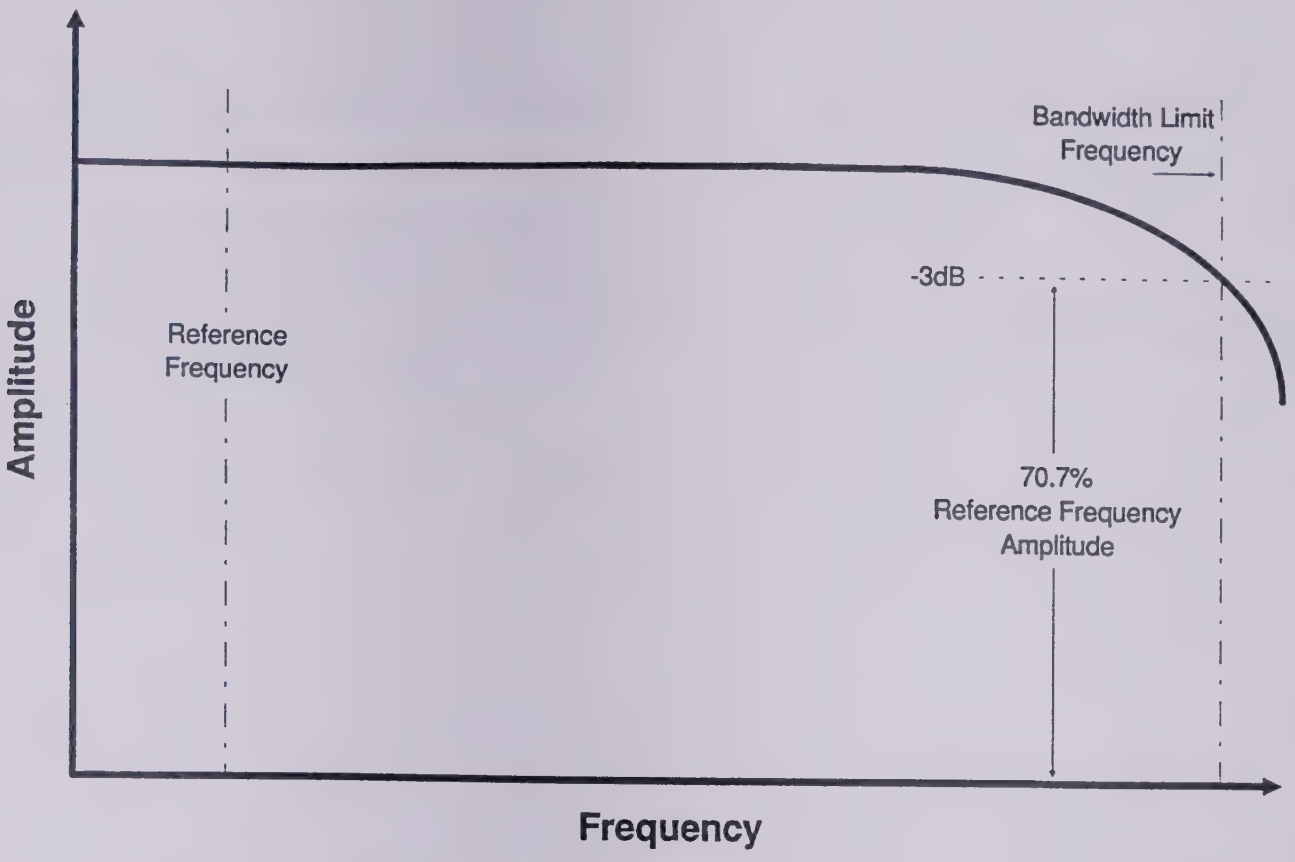
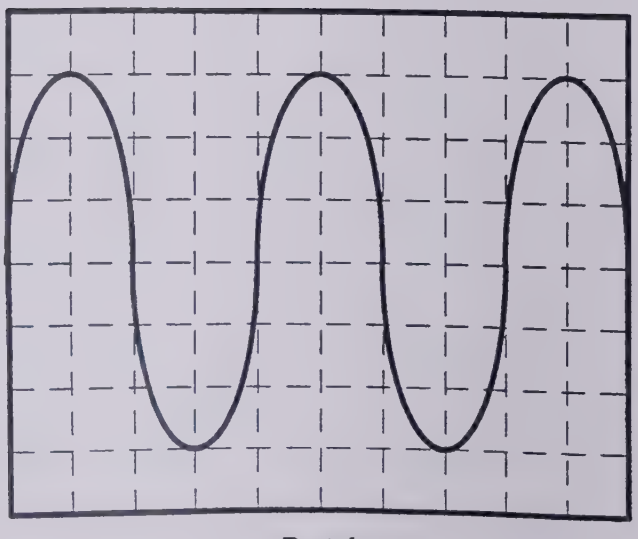
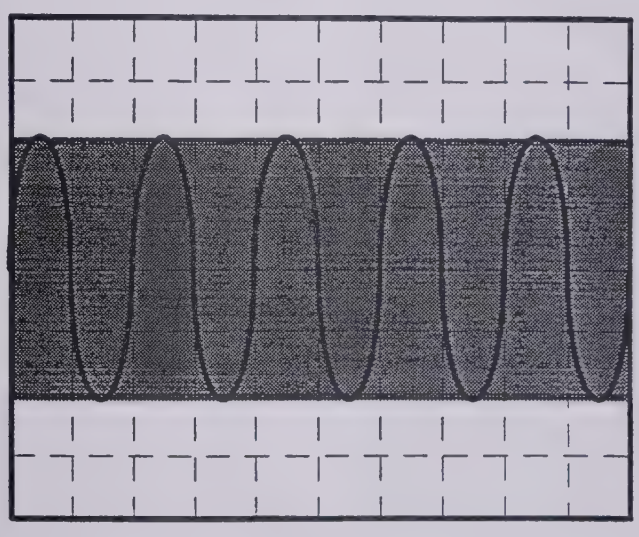


FIGURE 2-3: Bandpass Measurement



Part A
Set the Reference Amplitude

FIGURE 2-4: Reference Setup



Part B
Find the -3dB Point

FIGURE 2-5: The –3dB Point

In some applications, a wide bandwidth DVM can be substituted for the oscilloscope. The following procedure may be used.

1. Connect the DVM to the output of the DUT. Set the reference frequency amplitude first. Adjust the SG 5050 output amplitude and the DUT gain to show some convenient value on the DVM, such as 1 volt.

2. Next, slowly increase (or decrease) the SG 5050 frequency until the DVM reading is 70.7% of the reference amplitude. Do not adjust the gain or amplitude controls during this step.

3. Check the SG 5050 frequency readout display. This is the –3dB frequency of the DUT.

SECTION 3
PROGRAMMING

INTRODUCTION

This manual section provides the information required for programming the TEGAM SG 5050 Leveled Sine Wave Generator through the IEEE-488 bus, commonly called the General Purpose Interface Bus (GPIB). The IEEE-488 bus interface is specified and described in the IEEE-Standard 488.1-1987, Standard Digital Interface for Programmable Instrumentation.[1]

The information in this section assumes that the reader is knowledgeable in IEEE-488 bus communication and has some experience in programming a system that uses a GPIB-style interface.

All TEGAM programmable TM 5000 instruments are designed to communicate with any controller that can send and receive ASCII messages (commands) over the IEEE-488 bus. The instruments are connected to the IEEE-488 bus through a TM 5000 power module. Refer to the Operating Instructions section of this manual for information on installing the SG 5050 in the power module. Also, it is helpful to review that section and become familiar with front panel functions.

Commands for TM 5000 programmable instruments either alter instrument settings or request information from the instrument. The command set for each instrument is designed for compatibility between TM 5000 instrument types. When possible, the same commands are used in different instruments to control similar functions. In addition, commands are specified in mnemonics that are related to the functions implemented. For example, the INIT command initializes instrument settings to predefined default settings.

[1] Published by the Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, NY 10017.

IEEE-488 INTERFACE FUNCTION SUBSETS

The SG 5050 IEEE-488 interface is based on the IEEE-488.1-1987 interface (described above).

Table 3-1 shows the compatibility of SG 5050 operation with these combined standards.

Table 3-1: IEEE-488 Interface Function Capability

Function	Subset	Capability
Source Handshake	SH1	Complete Capability
Acceptor Handshake	AH1	Complete Capability
Basic Talker	T6	Responds to serial poll. Untalks if My Listen Address (MLA) is received.
Basic Listener	L4	Unlistens if My Talk Address (MTA) is received.
Service Request	SR1	Complete Capability
Remote-Local	RL1	Complete Capability
Parallel Poll	PP0	Does not respond to Parallel Poll

Device Clear	DC1	Complete Capability
Device Trigger	DT0	Does not respond to GET
Controller Function	C0	No controller function

GPIB Address and Message Terminator

The SG 5050 primary GPIB address can be set to any decimal number in the range 0 to 31. Address 31 effectively removes the SG 5050 from the bus, though it remains an electrical load. The SG 5050 is shipped with the GPIB address set to 10.

The SG 5050 responds to one of two possible message terminators (LF and EOI or EOI only). The message terminator must match that required by the controller. The SG 5050 is shipped with the message terminator set to EOI only. The message terminator and the primary GPIB address are stored in nonvolatile RAM memory.

The front panel SPCL button allows the current GPIB primary address and message terminator to be displayed on the SG 5050 readout. To display the GPIB address, press the SPCL button, enter 240 from the keypad, and press ENTER. The address is then displayed, for example, `GPIB 10`. Pressing the ID button will also display the GPIB address.

To display the message terminator, press the SPCL button, enter 241 from the keypad, and press ENTER. The letters `LF EOI` are then displayed if the selected message terminator is LF EOI, and the letters `EOI` are displayed if the terminator is EOI only.

Resetting the GPIB Address and Message Terminator

The SPCL button can also be used to change the GPIB primary address and the message terminator. To reset the GPIB address, perform the following operation:

1. Press SPCL.
2. Enter 240 from the keypad.
3. Press ENTER.
4. After current GPIB address setting is displayed, enter the new address from the keypad.
5. Press ENTER.

To reset the message terminator, perform the following operation:

1. Press SPCL.
2. Enter 241 from the keypad.
3. Press ENTER.
4. After current message terminator is displayed, use the knob to select the new terminator.
5. Press ENTER.

COMMANDS

The SG 5050 is controlled either by front panel controls or by remote commands that it receives from the controller through the GPIB interface. The remote commands are divided into three types:

- **Setting commands** – control instrument settings.
- **Query/Output commands** – request data.
- **Operational commands** – changes instrument operational commands (i.e., store, test, etc.).

When the instrument is in the remote state, it executes all three types of commands in the appropriate manner (for example, sets an

instrument control or returns the requested data). In the local state (that is, when the instrument is under front panel control), the instrument only executes query/output commands.

In the following sections, the SG 5050 commands are presented in three ways:

- **Command Summary** – A command list divided into functional groups, with brief descriptions of each command.
- **Control/Command Descriptions** – A front panel illustration showing command relationships to front panel operation and internal parameters.
- **Detailed Command Descriptions** – An alphabetically arranged presentation of all the commands with complete detailed descriptions.

Command Format

A command consists of a header, and if necessary, one or more arguments. The command headers are English-language words that denote the operation to be carried out, such as INIT (initialize the instrument), or FREQUENCY (set the output signal frequency). Only the first three characters of a command header must be given, although it is acceptable to enter the entire command header.

When a command requires arguments, they are entered after the command header. For example, the FREQUENCY command requires an argument to give the desired frequency setting (`FRE 15000`). A space character generally separates the header and arguments, although the command will be accepted without the space.

The headers for query commands include a terminating question mark (?) symbol (`USEREQ?`). Since only the first three characters of a command header must be given, the ? may be given after these characters (for example, (`USE?`).

Additional information about the command format is given in the section titled Message Format.

Command Summary

This section provides a summary of the SG 5050 commands. The list is arranged in functional groups: instrument commands, status commands and system commands.

NOTE

Capitalized letters in the command header word are required characters; the lower case characters may be optionally entered. Angle brackets < > indicate a required user supplied element. Square brackets [ ] indicate an optional element.

Instrument Commands

The following commands control instrument operations that are associated with front panel controls.

`AMPlitude <num> [:<dBm>]` – sets the amplitude of the output signal. The default units are volts, if desired, dBm can be selected.

`AMPlitude?` – Returns the current amplitude setting.

`FREquency <num>` - Sets the frequency of the output signal.

`SREFreq <num>` – Sets the value of the reference frequency.

`FREquency?` – Returns the current frequency setting.

`REFreq ON` – Turns on the 50KHz reference frequency and sends it to the output.
`REFreq OFF` – Turns off the 50KHz reference frequency and enables the variable frequency controls.

REFreq? – Returns the current status of the reference frequency (REFREQ ON or OFF).

OUTput ON – Turns the output on.

OUTput OFF – Turns the output off.

OUTput? – Returns the current status of the output (OUTPUT ON or OFF).

STOre <num> - Stores the current front panel setup at location 1 to 20.

RECall <num> - Recalls the front panel setup from location 0 to 20. (Location 0 contains the initialization settings.)

Status Commands

The following commands enable and disable service requests and return status information about instrument operation.

RQS ON – Enables generation of service requests.

RQS OFF – Disables generation of service requests.

RQS? – Returns status of service requests (RQS ON or OFF).

USEreq ON – Enables SRQ operation when the ID button is pushed.

USEreq OFF – Disables SRQ operation when the ID button is pushed.

USEreq? – Returns status of user request (USEREQ ON or OFF).

LEVeled? – Returns current status of output signal (LEVELED YES or NO).

EXTtb? – Returns current status of the external timebase input (EXTTB ACTIVE or INACTIVE).

System Commands

The following commands perform system wide operations.

ID? – Returns instrument identification and firmware version.

INIt – Initializes instrument settings.

SET? – Returns the current instrument settings to the GPIB interface. This command can be used for storage of setups on the host controller for later retrieval. It can also be used during development of an automated test procedure by allowing the host controller to "learn" a series of manual front panel settings.

TESt – Initiates a self-test on the instrument. When the test is complete, the instrument returns to the settings last entered. If the self-test failed, the SG 5050 returns an SRQ to the controller.

EVEnt? or ERRor? – Returns information about the event reported in the last serial poll.

HELp? – Returns a list of all the command headers the SG 5050 accepts.

ABStouch <nrl> - Provides a means of remotely activating (touching) front panel buttons and controls through the GPIB interface. Refer to Table 3-2.

CAL? – Returns a list of all the calibration settings (SPCL 99) stored in NVRAM.

Control/Command Descriptions

Figure 3-1 shows the instrument commands and their relationship to the front panel controls.

Detailed Command List

The following section provides a detailed description of the SG 5050 commands and their command syntax.

NOTE

Capitalized letters in the command header word are required characters; the lower case characters may be optionally entered. Angle brackets < > indicate a required user supplied element. Square brackets [ ] indicated an optional element.

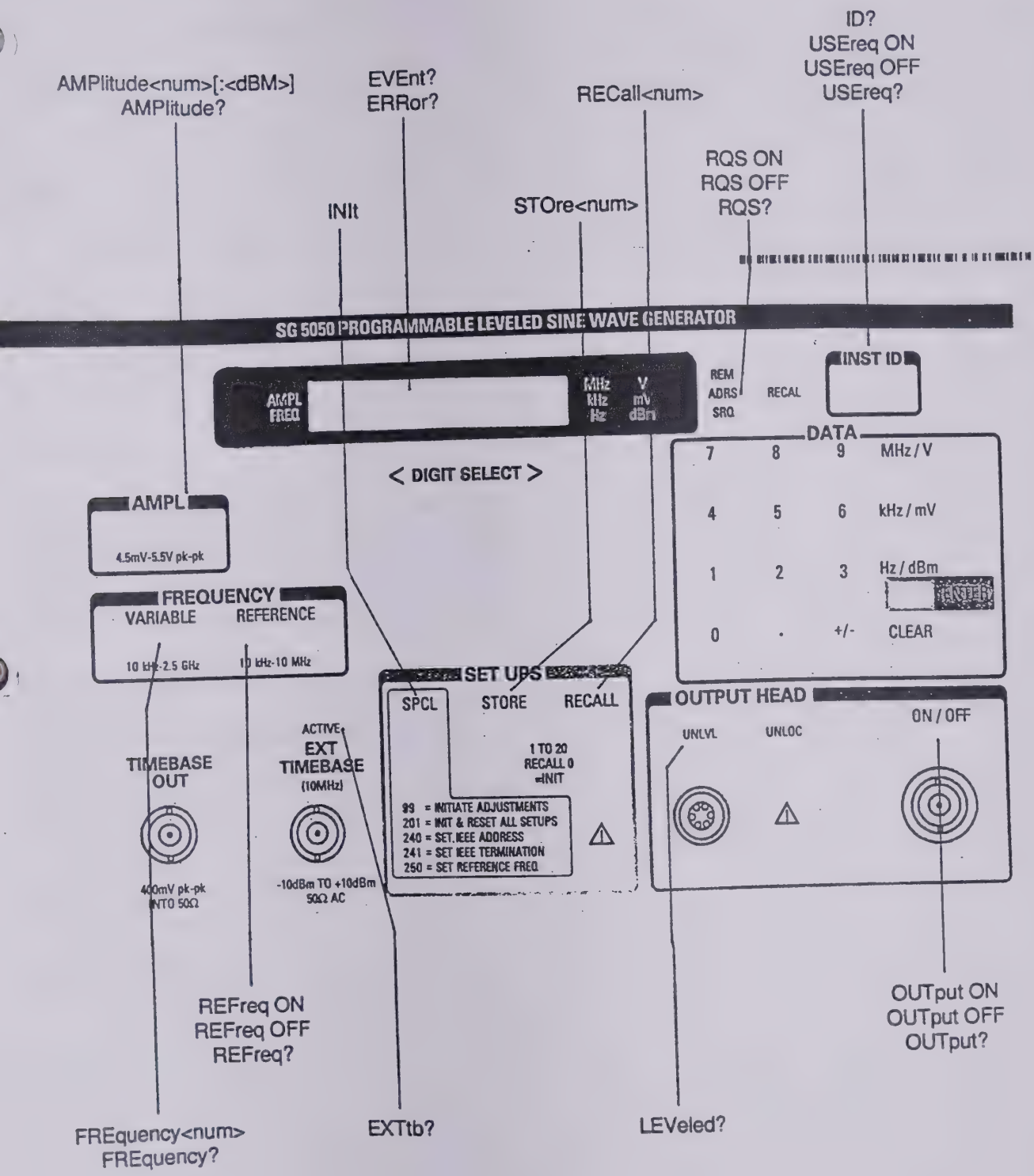


FIGURE 3-1: Instrument Commands and Front Panel Controls

ABSTOUCH

Type:

Setting

Setting Syntax:

```
ABStouch <nrl>
```

Examples:

```
ABSTOUCH 5
ABS 5
```

Discussion:

This command causes one or more front panel buttons or controls to be remotely activated (touched) through the GPIB interface. This feature is useful for evaluation and applications procedures that simulate operator actions.

Table 3-2: ABSTOUCH Command Arguments

Front Panel Switch Function	Argument (decimal number)
Knob Increment	0
Knob Decrement	1
Output ON	2
CLEAR	3
0	4
.	5
+/-	6
Hz/dBm/ENTER	7
1	8
2	9
3	10
KHz/mV	11
4	12
5	13
6	14
MHz/V	15
7	16
8	17
9	18
INST ID	19
AMPLITUDE	20
VARIABLE	21
STORE	22
SPCL	23
<	24
>	25
REFERENCE	26
RECALL	27

AMPLITUDE

Type:

Setting or query

Setting Syntax:

```
AMPlitude <num> [:dBm]
```

Examples:	**Amplitude Selected:**
`AMPLITUDE 4.5`	4.5V p-p
`AMPL .5`	500Mv P-P
`AMP 3.5E-2`	35mV p-p
`AMP 0:dBm`	0dBm
`AMP -30:dBm`	-30dBm

Query Syntax:

```
AMPlitude?
```

Query Response Syntax:

```
AMPLITUDE <num>
AMPLITUDE <num> :dBm
```

Query Response Examples:

```
AMPLITUDE 3.250
AMPLITUDE 400.OE-3
AMPLITUDE -15.00:DBM
```

Discussion:

This command sets the amplitude of the output signal in volts peak-to-peak or dBm. If dBm units are not specified, volts are assumed. The dBm range is –42.95dBm to +18.75dBm, with a resolution of 0.05dBm. The voltage peak-to-peak range of the instrument is 4.50mV to 5.500V. This range is divided into three subranges, and the amplitude resolution is different in each of these subranges as follows:

Range	**Resolution**
-42.95dBm to +18.75dBm	0.05dBm
4.50mV to 55.00mV	0.02mV
55.2mV to 550.0mV	0.2mV
0.552V to 5.500V	2mV

If the amplitude specified in the command has a greater resolution than the subrange it falls in, the amplitude is rounded off to the closest allowable resolution.

The `AMPlitude?` Command causes the current amplitude setting to be returned.

CAL?

Type:

Query

Query Syntax:

```
CAL <num>,<num>,<num>,
<num>,<num>,<num>,<num>,
<num>,<num>,<num>,<num>,
<num>,
```

Query Response Examples:

```
CAL 139,136,140,2746,2755,
2747,2838,340,2843,341,
2841,342
```

Discussion:

This query returns the current DAC settings stored in NVRAM that were set either by default or by selection of the SPCL 99 calibration routine. Table 3-3 below shows a list of the DACs and the name of each DAC setting, listed in the order returned by the CAL? Query.

Table 3-3: DAC Setting Names

DAC Name	DAC Setting Name
Offset DAC (high byte)	lf_power_amp_offset
Offset DAC (low byte)	lf_preamp_offset
Offset DAC (high byte)	rf_power_amp_offset
LF Level DAC	lf_gain_cal_x1
LF Level DAC	lf_gain_cal_x10
LF Level DAC	lf_gain_cal_x100
RF Level DAC	rf_gain_max_x1
RF Level DAC	rf_gain_min_x1
RF Level DAC	rf_gain_max_x10
RF Level DAC	rf_gain_min_x10
RF Level DAC	rf_gain_max_x100
RF Level DAC	rf_gain_min_x100

ERROR?
EVENT?

Type:

Query

Query Syntax:

```
ERRor?
EVEnt?
```

Query Response Syntax:

```
ERROR <num>
EVENT <num>
```

Query Response Examples:

```
ERROR 205
EVENT 351
```

Discussion:

These commands return information about the event reported in the last serial poll. If RQS is ON, the <num> response for both commands is the event code for the last reported status byte. If RQS is OFF, <num> is the event code for the highest priority event that has occurred. The event code will be cleared upon completion of these commands. Refer to the section titled Status and Error Reporting for a discussion of event codes and status bytes. Table 3-4 lists all the SG 5050 error/event codes.

These two commands are equivalent and either may be used to preserve compatibility with other TEGAM GPIB products.

EXTTB?

Type:

Query

Query Syntax:

```
EXTtb?
```

Query Response (one of the following):

```
EXTTB ACTIVE
EXTTB INACTIVE
```

Discussion:

This command returns the current status (ACTIVE or INACTIVE) of the external timebase input (EXT TIMEBASE) connector).

FREQUENCY

Type:

Setting or query

Setting Syntax:

```
FREquency <num>
```

Examples:

```
FREQUENCY 120E3
FREQ 1.5E4
FRE 5E+4
FRE .9
```

Query Syntax:

```
FREquency?
```

Query Response Syntax:

```
FREQUENCY <num>
```

Query Response Examples:

```
FREQUENCY 125.00E+3
FREQUENCY 1.0000E+3
```

Discussion:

This command sets the frequency of the output signal. The frequency range of the instrument is 10KHz to 2.500GHz. This range is divided into three subranges, and the frequency resolution is different in each of these subranges as follows:

Range	Resolution
10.000KHz to 49.999KHz	1Hz
50.00KHz to 550.00000MHz	10Hz
550.00000MHz to 1.500GHz	100Hz
1.500GHz to 2.500GHz	1000Hz

HELP?

Type:

Query

Query Syntax:

```
HELp?
```

Query Response:

```
HELP ABSTOUCH,AMPLITUDE,
CAL,ERROR,EVENT,EXTTB,
FREQUENCY,HELP,ID,INIT,
LEVELED,OUTPUT,RECALL,
REFREQ,RQS,SET,SREFREQ,
STORE,TEST,USEREQ
```

Discussion:

This command returns the word HELP followed by a list of all the command headers the SG 5050 accepts.

ID?

Type:

Query

Query Syntax:

```
ID?
```

Query Response:

```
ID TEGAM/SG5050,Vxx.x,Fx.x
```

Discussion:

This command returns the instrument identification and the firmware version as follows:

TEGAM/SG5050 – identifies the instrument type.

Vxx.x – identifies the version of the TEGAM main processor firmware.

Fx.x – identifies the instrument's RF deck processor firmware version. For example, F1.0 indicates the firmware version 1.0.

INIT

Type:

System

Setting Syntax:

```
INIt
```

Example:

```
INIT
```

Discussion:

The INIT command clears the current settings and initializes the SG 5050 to the following predefined settings:

```
OUTPUT OFF
AMPLITUDE 1.000
FREQUENCY 1.00000E+7
REFREQ OFF
RQS ON
USEREQ OFF
SREFREQ 50.0E6
```

After the SG 5050 has executed the INIT command, the display shows FREQ 10.00000MHz, and the switch button VARIABLE is illuminated. (No other switches are illuminated.)

This command has the same effect as the RECALL 0 command. Neither of these commands affects the UNLVL or EXT TIMEBASE Active LED. The stored settings buffer is not affected.

LEVELED?

Type:

Query

Query Syntax:

```
LEVeled?
```

Query Response (one of the following):

```
LEVELED YES
LEVELED NO
```

Discussion:

This command returns the leveled-signal status of the output signal (YES or NO).

OUTPUT

Type:

Setting or query

Setting Syntax:

```
OUTput ON
OUTput OFF
```

Examples:

```
OUTPUT ON
OUTPUT OFF
```

Query Syntax:

```
OUTput?
```

Query Response (one of the following):

```
OUTPUT ON
OUTPUT OFF
```

Discussion:

This command turns the signal output on or off at the OUTPUT HEAD connectors, depending on the argument specified. The source impedance is maintained when the output is off. At power-up, the output is set to OFF.

The `OUTput?` Command returns the current status of the output signal (ON or OFF).

RECALL

Type:

Operational

Syntax:

```
RECall
```

Examples:

```
RECALL 2
REC 7
REC 0
```

Discussion:

This command recalls the instrument settings from the nonvolatile RAM location specified in the <num> argument and sets the instrument to those settings. The <num> argument can be from 0 to 20 (decimal). Numbers 1 through 20 are used for user-selectable setups; number 0 references the initialization setup (that is, the `RECALL 0` command is equivalent to the INIT command). If no settings are stored in the specified location, the instrument assumes the `INIT` command settings.

REFREQ

Type:

Setting or query

Setting Syntax:

```
REFreq ON
REFreq OFF
```

Query Syntax:

```
REFreq?
```

Query Response (one of the following):

```
REFREQ ON
REFREQ OFF
```

Discussion:

This command turns the 50KHz reference frequency ON and OFF. When the reference frequency is ON, the variable frequency controls are disabled and the reference frequency is connected to the output. When the reference frequency is OFF, the variable frequency controls are enabled and control the frequency of the output signal. The output frequency is returned to the previous variable frequency. The output amplitude remains at its last setting.

The REFreq? Command returns the current status of the reference frequency (ON or OFF).

RQS

Type:

Setting or query

Setting Syntax:

```
RQS ON
RQS OFF
```

Query Syntax:

```
RQS?
```

Query Response (one of the following):

```
RQS ON
RQS OFF
```

Discussion:

This command enables and disables the instrument's ability to generate service requests (SRQs). When RQS (request for service) is ON, the instrument asserts an SRQ on the GPIB whenever an event occurs that requires a service request. The events that normally cause service requests to be asserted include the power-up sequence, self-test errors, front panel operation errors, programming errors and internal errors.

When RQS is OFF, SRQs are saved, and the SRQ annunciator light on the instrument front panel is lit. An ERROR? Or EVENT? Command query can then be used to determine which SRQs have been generated.

The RQS? Command returns the current status of the SRQ function (ON or OFF).

SET?

Type:

Query

Query Syntax:

```
SET?
```

Query Response Example:

```
OUTPUT ON; AMPLITUDE
17.40E-3;FREQUENCY
123.34543E+6;REFREQ OFF; RQS
ON; USEREQ OFF;
SREFREQ10.00000E6
```

Discussion:

This command returns the current instrument settings for OUTPUT (ON or OFF), AMPLITUDE, FREQUENCY, REFREQ (ON or OFF), RQS (ON or OFF), USEREQ (ON or OFF), and the value of the reference frequency. The maximum length of the settings query data string is 103 bytes.

SREFREQ

Type:

Setting or Query

Setting Syntax:

```
SREfreq <num>
```

Examples:

```
SREFREQ 1.0E6
SREF 1.5E4
```

Query Syntax:

```
SREfreq?
```

Query Response Syntax:

```
SREFREQ <num>
```

Query Response Examples:

```
SREFREQ 50.00E3
SREFREQ 4.00000E6
```

Discussion:

This command sets the frequency of the output signal when the reference frequency is active. The frequency range of the reference signal is 10KHz to 10MHz. The frequency resolution is the same as the frequency setting for each subrange.

STORE

Type:

Operational

Syntax:

```
STOre <num>
```

Examples::

```
STORE 8
STO 13
```

Discussion:

This command causes the current instrument front panel control settings to be stored in nonvolatile RAM at a location specified with the <num> argument. The <num> argument can be from 1 to 20 (decimal). 20 front panel control settings are saved for each instrument setup. Nonvolatile RAM is provided so that the settings are saved when power is turned off to the instrument.

TEST

Type:

Operational

Syntax:

```
TESt
```

Example:

```
TEST
```

Discussion:

This command causes the instrument to perform a self-test. When the test is complete, the instrument returns to the settings last entered. If the self-test failed, the SG 5050 returns an SRQ to the controller.

USEREQ

Type:

Setting or query

Setting Syntax:

```
USEreq ON
USEreq OFF
```

Examples:

```
USEREQ ON
USEREQ OFF
```

Query Syntax:

```
USEreq?
```

Query Response (one of the following):

```
USEREQ ON
USEREQ OFF
```

Discussion:

This command enables or disables the SRQ interrupt that is generated when the front panel INST ID button is pressed. When the USEREQ (user request) function is OFF, the instrument is inhibited from returning the instrument ID SRQ when the INST ID button is pressed.

The USEreq? command returns the current status of the instrument ID SRQ (ON or OFF).

B7 B6 B5 / BITS / B4 B3 B2 B1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		NUMBERS SYMBOLS		UPPER CASE		LOWER CASE	
0 0 0 0	0 NUL 0	20 DLE 16	40 SP 32	60 0 48	100 @ 64	120 P 80	140 ` 96	160 p 112
0 0 0 1	1 GTL SOH 1	21 LLO DC1 17	41 ! 33	61 1 49	101 A 65	121 Q 81	141 a 97	161 q 113
0 0 1 0	2 STX 2	22 DC2 18	42 " 34	62 2 50	102 B 66	122 R 82	142 b 98	162 r 114
0 0 1 1	3 ETX 3	23 DC3 19	43 # 35	63 3 51	103 C 67	123 S 83	143 c 99	163 s 115
0 1 0 0	4 SDC EOT 4	24 DCL DC4 20	44 $ 36	64 4 52	104 D 68	124 T 84	144 d 100	164 t 116
0 1 0 1	5 PPC ENQ 5	25 PPU NAK 21	45 % 37	65 5 53	105 E 69	125 U 85	145 e 101	165 u 117
0 1 1 0	6 ACK 6	26 SYN 22	46 & 38	66 6 54	106 F 70	126 V 86	146 f 102	166 v 118
0 1 1 1	7 BEL 7	27 ETB 23	47 ' 39	67 7 55	107 G 71	127 W 87	147 g 103	167 w 119
1 0 0 0	10 GET BS 8	30 SPE CAN 24	50 (40	70 8 56	110 H 72	130 X 88	150 h 104	170 x 120
1 0 0 1	11 TCT HT 9	31 SPD EM 25	51) 41	71 9 57	111 I 73	131 Y 89	151 i 105	171 y 121
1 0 1 0	12 LF A 10	32 SUB 26	52 * 42	72 : 58	112 J 74	132 Z 90	152 j 106	172 z 122
1 0 1 1	13 VT B 11	33 ESC 27	53 + 43	73 ; 59	113 K 75	133 [91	153 k 107	173 { 123
1 1 0 0	14 FF C 12	34 FS 28	54 , 44	74 < 60	114 L 76	134 \ 92	154 l 108	174 | 124
1 1 0 1	15 CR D 13	35 GS 29	55 - 45	75 = 61	115 M 77	135] 93	155 m 109	175 } 125
1 1 1 0	16 SO E 14	36 RS 30	56 . 46	76 > 62	116 N 78	136 ^ 94	156 n 110	176 ~ 126
1 1 1 1	17 SI F 15	37 US 31	57 / 47	77 UNL ? 63	117 O 79	137 UNT _ 95	157 o 111	177 DEL (RUBOUT) 127
	ADDRESSED COMMANDS	UNIVERSAL COMMANDS	LISTEN ADDRESSES		TALK ADDRESSES		SECONDARY ADDRESSES OR COMMANDS (PPE)	(PPD)

KEY

octal 25 PPU — GPIB code
NAK — ASCII character
hex 15 21 — decimal

FIGURE 3-2: ASCII Character Chart

MESSAGES AND COMMUNICATION PROTOCOL

Command Separator

A message consists of a command or a series of commands followed by a message terminator. Messages consisting of multiple commands must have the commands separated by semicolons. A semicolon at the end of a message is optional. For example, each line below is a message:

```
INIT

INIT;RQS                    ON;USER
OFF;ID?;SET?

init;
```

Message Terminator

Messages may be terminated with EOI (the GPIB End-Or-Identify signal) or the ASCII line feed (LF) character. Some controllers assert EOI concurrently with the last data byte; others use only the LF character as a terminator. The SG 5050 can be set via the front panel to accept either terminator. With EOI only selected as the terminator, the instrument interprets any data byte received with EOI asserted as the end of an input message; it also asserts EOI concurrently with the last byte of an output message. With LFEOI selected as the terminator, the SG 5050 interprets either an LF character or EOI as a message terminator. Here, the instrument interprets the LF character without EOI asserted (or any data byte received with EOI asserted) as the end of an input message. To terminate output messages, the instrument transmits a carriage return (CR) followed by an LF character with EOI asserted. The SG 5050 is shipped with EOI only selected.

Formatting a Message

Commands sent to the SG 5050 must have the proper format (syntax) to be understood, however, this format is flexible in that variations are acceptable. The following describes this format and the acceptable variations.

The instrument expects all commands to be encoded in ASCII, however, it accepts both upper and lower case ASCII characters. All data output is in upper case (see Figure 3-2).

As previously discussed, a command consists of a header followed, if necessary, by arguments. A command with arguments may have a header delimiter, which consists of the space character (SP) between the header and the argument.

The SG 5050 ignores extra formatting characters SP that are added between the header delimiter and the argument, as shown in the following examples. (In these examples, the formatting characters are shown inside parenthesis.)

Example 1: `RQS(SP)ON;`

Example 2: `RQS(SPSP)ON;`

Example 3: `RQSON`

In general, these formatting characters are ignored after any delimiter and at the beginning and end of a message.

- (SP)RQS(SP)ON(CRLF)
- (SP)USER(SP)OFF

Number Formats

The SG 5050 recognizes the following three number formats:

- **NR1 (integer)** – Signed or unsigned decimal integers (for example, +0, -0, +1, 2, -1, -10).

- **NR2 (real)** – Signed or unsigned decimal real numbers (for example, -3.2, +5.0, .2).
- **NR3 (floating point)** – Floating point numbers expressed in scientific notation (for example, +1.0E-2, 1.47E1, 1.E-2, 0.01E+0).

In each of these formats, an unsigned value is interpreted as a positive value (that is, 2 is equivalent to +2).

Rounding of Numeric Arguments

The SG 5050 rounds numeric arguments to the nearest unit of resolution and then checks for out-of-range conditions. If the argument is outside the allowable range, the instrument sets the value to the highest (or lowest) allowable value within the range. For example, if a frequency of 2600MHz is given, the instrument frequency is set to 2500MHz, the maximum allowable frequency and an error 205 (argument out of range) is generated.

Message Protocol

As the SG 5050 receives a message it is stored in the input buffer, processed, and executed. Processing a message consists of decoding commands, detecting delimiters, and checking syntax. If an error is detected during processing, the instrument will assert SRQ.

Executing a message consists of performing the actions specified by its command(s). For setting commands, this involves updating the instrument settings. The setting commands are executed in order received. Execution of the settings occurs when the instrument has received enough characters of the command to determine a valid setting. The instrument requires a message terminator to execute a valid command.

The SG 5050 behaves the same regardless of whether each command is sent as a separate message or several commands are included in one message. The only difference is that multiple-command messages require less bus overhead.

When the SG 5050 receives a query/output command in a message, it executes the command by retrieving the appropriate data and putting it in the output buffer. The instrument then continues to process and execute the remainder of the commands in the message. The query data is sent to the controller when the SG 5050 is made a talker.

NOTE

It is not recommended that multiple queries be placed in one message. If more than one query is in a message, one or more response(s) may be lost. No error message will be generated.

Multiple Messages

The SG 5050 input buffer has finite capacity and a single message may be long enough to fill it. In this case, the instrument will process the first portion of the message before the instrument accepts additional input. While the commands in the full input buffer are being processed, the instrument holds off additional data (by asserting NRFD) until space is available in the input buffer.

When space is available, the instrument can accept the next message before the first has been completely processed.

As described above, after the SG 5050 executes a query output command in a message, it holds the response in its output buffer until the controller makes the instrument a talker. If the instrument receives a new message before all of the output from the previous message is read, it clears the output buffer before executing the new message. This prevents the controller from getting unwanted data from old messages.

One other situation can cause the SG 5050 to delete output. The execution of a long message might cause both the input and output buffers to become full. When this occurs, the instrument cannot finish execution of the message because it

is waiting for the controller to read the data it has generated; but the controller cannot read the data because it is waiting to finish sending its message. Because the instrument's input buffer is full and it is holding off the rest of the controller's message with NRFD, the system hangs up with the controller and instrument waiting for each other. When the SG 5050 detects this condition, it generates an error, asserts SRQ and deletes the data in the output buffer.

Instrument Responses to IEEE-488 Interface Messages

The IEEE-488.1-1987 bus standard defines a set of interface commands and the effects of those commands on the instrument's interface functions. This section describes the effects of the IEEE-488 interface messages on SG 5050 operation. The standard abbreviations for these commands are used here.

UNL (Unlisten) and UNT (Untalk)

The UNL command causes the SG 5050 listener function to go to its idle state (unaddressed). In the idle state, the instrument does not accept instrument commands from the IEEE-488 bus.

The UNT command causes the instrument talker function to go to its idle state. In this state, the instrument cannot supply output data via the bus.

The ADRS indicator is off when both the talker and listener functions are idle. If the SG 5050 is either talk-addressed or listen-addressed, the indicator is on.

IFC (Interface Clear)

The IFC command has the same effect as issuing both the UNT and UNL commands. The front panel ADRS indicator is off.

DCL (Device Clear)

The DCL command reinitializes communication between the SG 5050 and its controller. In response to DCL, the instrument clears any input and output messages. Also cleared are any errors or events waiting to be reported, except the power-on event. If the SRQ line is asserted for any reason other than power-on when DCL is received, SRQ is unasserted.

SDC (Selected Device Clear)

The SDC command has the same function as DCL, however, only instruments specifically addressed respond to SDC.

SPE (Serial Poll Enable)

The SPE command enables the SG 5050 to supply output serial poll status bytes when it is talk-addressed.

SPD (Serial Poll Disable)

The SPD command switches the SG 5050 to its normal operation of sending the data from the output buffer.

MLA (My Listen Address) and MTA (My Talk Address)

The SG 5050 IEEE-488 bus address establishes the primary listen and talk addresses. The current setting of the bus address is displayed on the instrument front panel readout window when the INST ID button is pressed. When the instrument is addressed to either talk or listen, the front panel ADRS indicator is lighted.

LLO (Local Lockout)

The LLO command causes the SG 5050 to change to a lockout state: from LOCS to LWLS or from REMS to RWLS. The LLO command sent by itself does not set the instrument into Local Lockout. You must send a following command to cause the GPIB circuitry to recognize and assert LLO.

REN (Remote Enable)

If REN is true, the SG 5050 will change to a remote state (from LOCS to REMS if the internal message return-to-local (rtl) is false, or from LWLS to RWLS when its listen address is received). REN false causes a transition from any state to LOCS; the instrument stays in LOCS as long as REN is false.

A REN transition might occur after message processing has started. In this case, execution of the message being processed is not affected by a transition.

GTL (Go To Local)

If the instrument is listen-addressed, the GTL command causes the SG 5050 to change to local state. Remote-to-local transitions caused by GTL do not affect the execution of the message being processed when GTL is received.

Remote-Local Operation

The preceding discussion of interface messages describes the state transitions that the GTL and REN commands cause. Most front panel controls cause a transition from REMS to LOCS by asserting a message called return-to-local (rtl). This transition might occur during message execution; but, in contrast to GTL and REN transitions, a transition initiated by rtl affects message execution. In this case, the instrument generates an error if there are any unexecuted setting or operational commands. Front panel controls that change only the display (such as INST ID) do not affect the remote-local states; only front panel controls that change settings assert rtl. The rtl message remains asserted while multiple keystroke settings are entered, and it is unasserted after the execution of the settings.

The SG 5050 maintains a record of its settings in the current settings buffer and new settings from the front panel or the controller update these recorded settings. In addition, the front panel is updated to reflect setting changes caused by commands. Instrument settings are unaffected by transitions between the four remote-local states. The REM indicator is lighted when the instrument is in REMS or RWLS.

Local State (LOCS)

In LOCS, the operator controls the SG 5050 settings via the front panel push buttons and knob. The only bus commands that are executed are those that do not change instrument settings (query-output commands). All other bus commands (setting and operational commands) generate an error since those functions are under front panel control.

Local Without Lockout State (LWLS)

When the SG 5050 is in LWLS, it operates the same as it does in LOCS, except that rtl does not inhibit a transition to remote.

Remote State (REMS)

In REMS, the SG 5050 executes all instrument commands from the GPIB bus. For commands having associated front panel indicators, the front panel is updated when the commands are executed.

Remote With Lockout State (RWLS)

In RWLS, the SG 5050 operates similar to REMS operation except that the rtl message is ignored. (The front panel is locked out.)

Status and Error Reporting

The SG 5050 can alert the controller that it requires service through the service request function (defined in the IEEE-488 Standard). The service request function also provides a means of indicating that an event (a change in status or an error) has occurred. To service a request, the controller performs a serial poll. In response to this poll, the SG 5050 returns a status byte (STB), which indicates whether or not it was requesting service. The STB can also provide a limited amount of information about the request. The format of the information encoded in the STB is given in Figure 3-3. Note that, when data bit 8 is set, the STB conveys device status information, which is contained in bits 1 through 4. (The SG 5050 does not utilize this feature.).

In case of an intermittent error condition, multiple SRQs may be stored in the SG 5050 internal stack. These SRQs can all be simultaneously cleared with a DCL (device clear) command.

NOTE

The SG 5050 status is available over the bus by serial and/or error query, with or without RQS on.

Because the STB conveys limited information about an event, the events are divided into classes, which the STB reports. The classes of events are defined as follows:

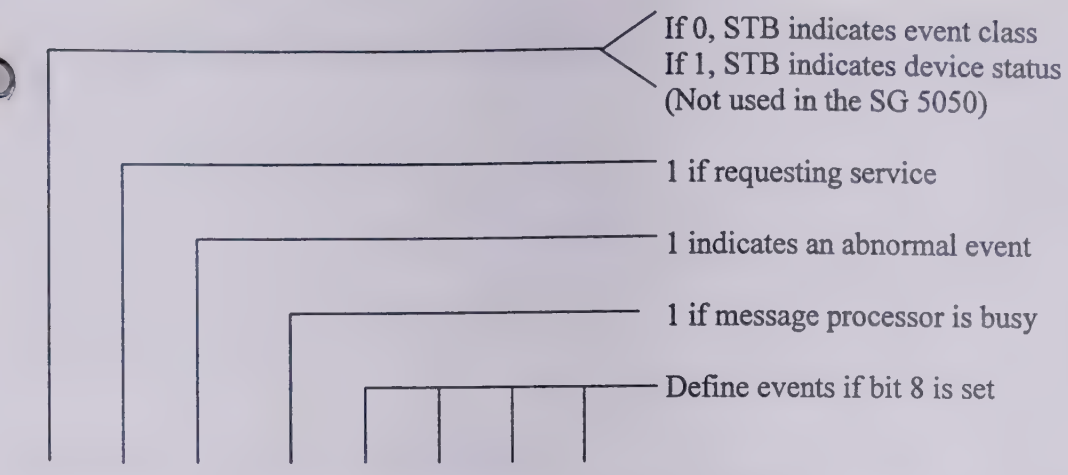
Command Error	Indicates that the SG 5050 has received a command that it cannot understand. The command does not affect the current state of the instrument.
Execution Error	Indicates that the instrument has received a command that it understands, but cannot execute because of the present state of the instrument, or because the command is out of the instrument's range.
Internal Error	Indicates that the instrument has detected a hardware condition or firmware problem that prevents operation.

Error Messages Sent to the Front Panel

Error messages sent to the front panel remain displayed until any front panel button is pushed or a GPIB command is executed.

An NVRAM battery test (E363) error means the battery backed up memory failed, resulting in the front panel setups and the GPIB address and message terminator information being lost. Front panel setups will default to the factory default settings with the GPIB address 10 and message terminator of EOI only.

An EEPROM error, CAL constants lost failure (E364) means the calibration constants are in some way not correct. The instrument then defaults to an output off mode and the front panel RECAL LED will be illuminated.


If 0, STB indicates event class
If 1, STB indicates device status
(Not used in the SG 5050)
1 if requesting service
1 indicates an abnormal event
1 if message processor is busy
Define events if bit 8 is set

8	7	6	5	4	3	2	1	BIT POSITION
128	64	32	16	8	4	2	1	DECIMAL WEIGHT
								Normal Events:
0	1	0	X	0	0	0	1	Power-up (65)
0	1	0	X	0	0	1	1	ID user request (67)
0	1	1	X	0	0	0	1	Abnormal Events:
0	1	1	X	0	0	1	0	Invalid command header (97)
0	1	1	X	0	0	1	1	Settings error (98)
								System error (99)

FIGURE 3-3: STB Bit Configuration

Bus Error/Event Codes and Serial Poll Response

The SG 5050 provides additional information about many of the events, particularly the errors reported in the STB. The controller can request the additional information by issuing an ERROR? or EVENT? command. In response, the SG 5050 returns a code that defines the event. These codes are described in Table 3-4.

Power-on Sequences and Settings

Each time power is applied to the SG 5050, the internal microprocessor performs a self-test diagnostic routine to check the instrument RAM and ROM functionality. If no RAM or ROM error is found, the microprocessor performs further routines that check the functionality of other instrument hardware.

If a functional failure is detected, an error code will appear in the display window. The error will remain displayed until cleared by pressing any front panel button or executing any GPIB command. The SG 5050 will respond to input and attempt to function in spite of the error. Refer to Table 3-4 for bus error codes and front panel error codes.

Upon successful completion of the self-tests, the SG 5050 restores the instrument settings that were in use when the instrument was last turned off, except that the sine wave signal to the output head will be turned off.

Table 3-4: Error Query and Status Responses

Description	Error/Event Query Response	Serial Poll (Decimal)[1]
Command Errors/Events		
System normal	0	NSB[2]
Command header error	101	97 or 113
Header delimiter error	102	97 or 113
Command argument error	103	97 or 113
Argument delimiter error	104	97 or 113
Non-numeric argument	105	97 or 113
Missing argument	106	97 or 113
Invalid message unit delimiter	107	97 or 113
Bad symbol	150	97 or 113
Syntax error	151	97 or 113
Symbol number too long	153	97 or 113
Invalid input character	154	97 or 113
Invalid string input	155	97 or 113
Numerical underflow	156	97 or 113
Execution Errors/Events		
Argument out of range	205	98 or 114
Not in adjustment mode	250	98 or 114
I/O buffers full, output flushed	251	98 or 114
Settings buffer empty	252	98 or 114
Illegal settings number specified	253	98 or 114

[1] If the message processor is busy, the instrument returns a number 16 (decimal) higher than the serial poll response.
[2] No Status Byte.

Beyond adjustment limit	254	98 or 114
Internal Errors/Events		
Interrupt fault	301	99 or 115
System error	302	99 or 115
HF unleveled	350	99 or 115
Reference loop unlocked	351	99 or 115
Wide loop unlocked	352	99 or 115
Narrow loop unlocked	353	99 or 115
Offset loop unlocked	354	99 or 115
DDS loop unlocked	355	99 or 115
Unplugged error	356	99 or 115
CPU Self-Test Errors		
EPROM checksum failure	360	99 or 115
NVRAM test failure	361	99 or 115
RAM test failure	362	99 or 115
NVRAM battery test failure	363	99 or 115
CAL constant checksum failure	364	99 or 115
Hardware Self-Test Errors		
Output OFF test failure	370	99 or 115
REF freq test failure	371	99 or 115
DDS OFF test failure	372	99 or 115
10.00000 MHz test failure	373	99 or 115
10.00001 MHz test failure	374	99 or 115
500.00000 MHz test failure	375	99 or 115
Wide loop divider test failure	376	99 or 115
Output amp powered test failure	377	99 or 115
System Errors/Event		
No errors or events	0	NSB
Power on	401	65 or 81
ID user request	403	67 or 83
SRQ pending	455	NSB

PROGRAMMING EXAMPLES

Talker/Listener Utility Programs

The following sample programs allow a user to send any of the commands listed in the Functional Command List and receive the data generated.

Talker/Listener Utility Program for IBM PC Compatibles

```
, ********************************************************************
, ******************* SG 5050 TALKER/LISTENER
PROGRAM**********************
, ********************************************************************
, THIS PROGRAM REQUIRES THAT THE SG 5050 ADDRESS BE SET TO THE
, FACTORY DEFAULT OF 10.
COMMON SHARED IBSTA%, IBERR%, IBCNT%
ID$ = "TEKDEV1"
CALL IBFIND (ID$, BD%)          , SELECT TEKDEVI FOR GPIB ACCESS
SG% = 10                        , SG% = FACTORY DEFAULT ADDRESS OF 10
CALL IBPAD (BD%, SG%)           , CHANGE TEKDEV1PRIMARY ADDRESS TO
ID$ = "GPIB0"                   , SET UP GPIB FOR BOARD LEVEL
CALL IBSRE (GP%, REMOTE%)       , COMMUNICATION
REMOTE% = 1
CALL IBSRE (GP%, REMOTE%)       , SET REMOTE ENABLE
CLS                             , CLEAR SCREEN
REPLY$ = SPACES$(125)           DIMENSION RD$ TO 125
PRINT
"********************************************************************"
PRINT "************** SG 5050 TALKER/LISTENER
PROGRAM**********************"
PRINT
"********************************************************************"
MAINPROG:
PRINT "RETURN TO EXIT; "
INPUT "ENTER MESSAGE(S)"L WRT$
IF WRT$ = " " THEN GOSUB TERMINATE
CALL IBWRT (BD%, WRT$)          , SEND MESSAGE TO SG 5050
GOSUB CHECKGPIB                 , CHECK FOR GPIB ERROR GOSUB
CHECKSG                         , GET SG 5050 ERROR MESSAGE
PRINT : PRINT "INSTRUMENT REPLY ", REPLY$
PRINT : PRINT "Returned status byte:'; SPR%,
PRINT : PRINT ERRM$
GOTO MAINPROG
, ********************************ERROR
ROUTINE**************************************
CHECKSG:
ERRM$ = SPACE$(50)
```

```
CALL IBRSP (BD%, SPR%)
CALL IBWRT (BD%, "ERR?")
CALL IBRD (BD%, ERRM$)
RETURN
CHECKGPIB:
IF IBSTA% >=0 AND BD% >=0 AND IBSTA% < &H4000 AND IBERR% <> 6 THEN
            RETURN' no error to report
IF BD% < 0 THEN PRINT "device not installed - use IBCONF then reboot"
IF IBSTA% > 0 AND IBSTA% >= &H4000 THEN PRINT "timeout"
IF BERR% = 6 THEN PRINT "timeout"
PRINTE "gpib error ", IBERR%
IF IBERR% =  0 THEN PRINT "DOS error device not installed"
IF IBERR% =  1 THEN PRINT "function requires GPIB-PC to be CIC"
IF IBERR% =  2 THEN PRINT "no listener on write function"
IF IBERR% =  3 THEN PRINT "GPIB-PC not addressed correctly"
IF IBERR% =  4 THEN PRINT "invalid argument to function call"
IF IBERR% =  5 THEN PRINT "GPIB-PC not system controller as required"
IF IBERR% =  6 THEN PRINT "I/O operation aborted"
IF IBERR% =  7 THEN PRINT "non-existent GPIB-PC board"
IF IBERR% = 10 THEN PRINT "I/O started before previous operation
completed"
IF IBERR% = 11 THEN PRINT "no capability for operation"
IF IBERR% = 12 THEN PRINT "file system error"
IF IBERR% = 14 THEN PRINT "command error during device call"
IF IBERR% = 15 THEN PRINT "serial poll status byte lost"
IF IBERR% = 16 THEN PRINT "SRQ stuck in ON position"
INPUT "[ENTER] TO CONTINUE"; A$     ' if help$ then
RETURN
, ********************************TERMINATE PROGRAM**********************
TERMINATE:
REMOTE% = 0
CALL IBSRE (GP%, REMOTE%)      , CLEAR REMOTE ENABLE
PRINT "PROGRAM TERMINATED."
END
```

SECTION 4
THEORY OF OPERATION

INTRODUCTION

This section of the manual describes the circuitry used in the SG 5050 Programmable Leveled Sine Wave Generator. The description begins with a discussion of the instrument, using the basic block diagram located in Section 9. Next, the major circuitry for each circuit board is described using detailed block diagrams, as necessary, to show the relationship between stages. Detailed schematic diagrams for each circuit are located in Section 9. at the back of this manual; refer to these schematics throughout the following circuit description for specific electrical values and relationships.

The logic convention (L) is used throughout the text in this section to denote and active Low signal.

SG 5050 OVERVIEW

The SG 5050 generates a high spectral purity sine wave whose amplitude is constant over a broad frequency range. In addition, both frequency and amplitude are programmable over the GPIB. The frequency range is 10KHz to 2500.00000MHz. The frequency setting resolution is 1Hz between 10.000KHz and 49.999KHz, 10Hz between 50.00KHz and 549.99999MHz. 100Hz between 550.0000MHz and 1499.9999MHz, and 1KHz between 1500.000MHz and 2500.000MHz. The output amplitude range is 4.5mV to 5.5V pk-to-pk (-42.95dBm to 18.75dBm, resolution 0.05dBm). The amplitude setting resolution is 0.02mV between 4.50mV and 55.00mV, 0.2mV between 55.2mV and 550.0mV, and 2mV between 552mV and 5.500 volts.

Frequency Control Operation

Two separate signal paths are used to generate the output sine wave, depending on the frequency selected. The Low Frequency (LF) signal covers the range of 10KHz to 25.000MHz. This signal is generated by the DDS (direct-digital synthesizer) and directly drives the LF Preamp and Output Amplifier. The High Frequency (HF) signal covers the range of 25.000MHz through 2500.000MHz. The HF signal is generated by a PLL (Phase Locked Loop), switchable VCOs and the DDS that is used to generate the PLL reference frequency. The PLL is programmed in large frequency steps and the DDS is programmed in fine steps to generate the specified frequency resolutions. The frequency accuracy of the SG 5050 is determined by the 10MHz Timebase Oscillator that directly or indirectly feeds all the frequency generator circuitry. This 10MHz Timebase Oscillator is voltage controllable and can be phase-locked to a precision external 10MHz reference for even greater frequency accuracy.

Amplitude Control Operation

Coarse control of the output amplitude is provided by the two 20db attenuators and the switchable amplifiers on the RF Amplifier Board. Two separate paths provide for control of the amplitude; one for 10KHz to 25.00000MHz (LF), and one for 25.00001MHz and 2500.000MHz (HF).

The LF amplitude is controlled through a variable gain amplifier (located on the DDS Board) and processor controlled D/A used to set output amplitude. The detection of output amplitude is performed by a precision rectifier on the RF Deck

assembly. The control uProcessor reads the output level and adjusts the amplifier gain accordingly.

The HF amplitude is controlled by a voltage variable 0-40db attenuator (VVA). The leveling head generates a DC signal that is proportional to peak output. This signal is read by the uProcessor and is used to control the VVA.

Front Panel and GPIB Operation

The SG 5050 receives commands to change its operation from either the front panel controls or from the GPIB. Once the instrument firmware accepts the command, the instrument is configured to the new setup. All front panel displays and controls communicate with the instrument through the CPU.

Internal Communications

The main processor (MC68306) and the uProcessor (68HC11) communicate over an opto-isolated asynchronous communications link through the A7 Interconnect Board. The 68HC11 communicates to the VCO (A3) and the RF Amp and Deck (A4-5) through a synchronous Serial Peripheral Interface (SPI) bus.

Hardware Diagnostics

The SG 5050 performs several diagnostic checks upon power up. If errors are detected, error messages will be shown in the readout display. See Table 3-3 in the Programming section for a complete list of the error codes that are shown in the readout display.

During normal operation, the various frequency and amplitude control loops will report an error to the CPU through the A7 Interconnect Board if a problem is detected. These errors will indicate a frequency loop not in lock or the HF amplitude leveling circuit cannot maintain amplitude leveling. These errors are also displayed on the readout display until cleared by pushing a key on the front panel.

BLOCK DIAGRAM DESCRIPTION

Eight circuit boards plus the amplitude leveling head comprise the SG 5050. The primary task of each circuit board is as follows:

A1 CPU Board

The CPU issues data and commands to the other circuit boards over the serial bus by way of the Interconnect Board and to the front panel display over the front panel interface ribbon cable.

A2 DDS Board

The A2 DDS Board contains the circuitry to control the fine resolution frequency for the HF mode and to directly generate and control the amplitude of the LF mode frequencies. This board also contains the 68HC11 processor that handles the detailed control of all hardware necessary to generate and output the precision sine wave signals.

A3 VCO Board

The A3 VCO Board contains the circuitry to generate the HF sine waves. This consists of a PLL and multiple VCOs that are switched in and out to generate specific frequency ranges.

A4 Output Deck Board

The A4 Output Deck Board contains the control and power supply circuitry necessary to support the A5 Amp and Filter Board and to control and power the A6 Leveling Head. It contains multiple power supplies to generate the programmable voltages used to control the Amp and Filter Board. It also contains the A/D converter used to detect the leveling head feedback signal and the

precision rectifier used to detect LF mode amplitude.

A5 Amp and Filter Board

The A5 Amp and Filter Board contains the circuitry to filter and amplify/attenuate the output signal to the proper level and purity. It consists of a multiband voltage controlled low-pass filter and a programmable set of amplifiers and attenuators to determine signal sources and flow to generate the proper LF and HF mode outputs.

A6 Leveling Head

The Leveling Head provides circuitry to detect the amplitude of the LF and HF amplitude. It also contains the precision 50Ω load. The leveling head is not field serviceable.

A7 Interconnect Board

The A7 Interconnect Board is used to distribute power from the various power supplies located on the A2 DDS Board and the A4 Output Board. This board also distributes the control lines used by the processor to configure the circuits as required for the various settings and functions.

A8 Front Panel Board

The A8 Front Panel Board contains the readout display used to indicate the current amplitude or frequency settings. This board also contains the control knob and push button switches used to set the frequency, set the amplitude, initiate the adjustment procedure, store or recall front panel setups, initialize all twenty front panel setups, or set the GPIB address and message terminator.

CIRCUIT THEORY NOTES

Frequency Synthesis

The SG 5050 develops its output frequency from a single 10MHz reference source using phase-locked loop techniques. A typical frequency synthesis loop is shown in Figure 4-0. The highly stable frequency reference, f_{REF}, is one input to the phase/frequency detector. The phase/frequency detector outputs an error correction voltage that drives the loop phase lock. Then under lock conditions the phase detector outputs narrow correction voltage pulses that are integrated by the Low Pass Filter generating a control voltage, V_C, which forces the voltage voltage-controlled oscillator (VCO) output frequency and phase to match that of the input reference. If there is a divider in the loop feedback path of divide ratio N, then the output frequency of the VCO is multiplied up in frequency by a factor of N. If the reference frequency is varied in small increments, then the output frequency will vary by an amount equal to $F_{REF\ VAR}$ x N. Since the DDS that generates the $F_{REF\ VAR}$ is programmable in .025Hz steps, the output can be varied in extremely fine increments to generate any specified frequency in the LF and HF mode. Even when N is large, the Output (e.g., 250 for 2500MHz), the output could still be resolved down to 250 x .025 or 7.25Hz.

Signal Power Notation

Since at high frequencies it is easier to measure power than voltage, the A5 RF Board schematics often show the signal level in terms of dBm. This notation refers to a power ratio compared to 1 milliwatt:

$$10 \log \left(\frac{P}{1mW} \right)$$

As an example, 0dBm represents 1mW, 10dBm represents 10mW, and 20dBm represents 100mW. It is possible to convert the dBm values into voltage into a specified load. In the typical case, the SG 5050 load resistance can be assumed to be 50 ohms. The equations that can be used to convert power in dBm to volts are shown below:

$$\text{XdBm} = 10 \log \left(\frac{P}{1mW} \right)$$

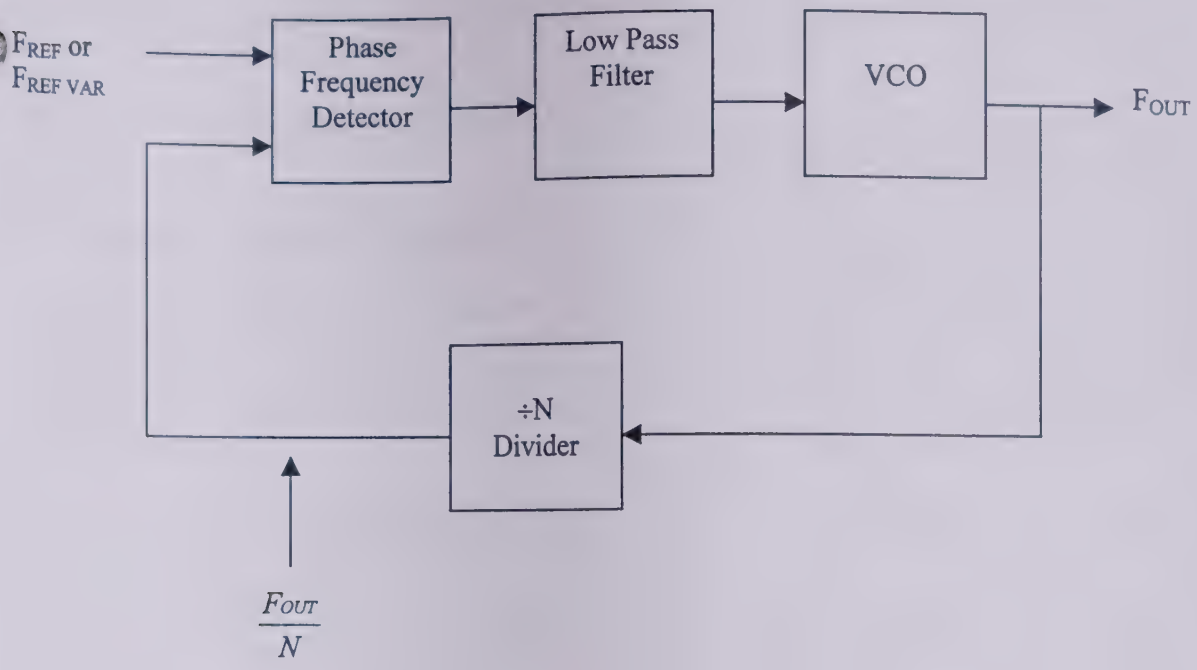
$$P = \frac{Vrms^2}{R_o} = \frac{Vrms^2}{50} \quad \text{for } R_o = 50 \text{ ohms}$$

$$Vpp = 2\sqrt{2}\ Vrms$$

$$Vpp = 20 \text{ X } 10^{\left(\frac{\frac{XdBm}{10}-3}{2}\right)}$$

ECL Signal Levels

Several of the frequency control circuits in the SG 5050 ECL integrated circuits are operated from a +5V supply rather than a more conventional –5.2V supply. This shifts the normal ECL logic levels. Using a +5V supply results in an ECL logic HI of about =4.1V and an ECL logic LO of about +3.3V. The threshold voltage, VB, under these conditions is about +3.7V. A threshold voltage supply is generated locally at several of the ECL ICs where the input signals are AC-coupled in order to minimize noise and reduce the effect of DC voltage offsets between circuit boards.



THE LOOP FEEDBACK FORCES

$$F_{REF} = \frac{F_{OUT}}{N}$$

OR

$$F_{REFVAR} = \frac{F_{OUT}}{N}$$

FIGURE 4-0: Frequency Synthesis Loop

DETAILED CIRCUIT DESCRIPTION

Refer to the schematic diagrams while reading this Detailed Circuit Description. Complete schematic diagrams are provided in the rear of this manual. The detailed Circuit Description subheadings provide schematic boxed numbers that refer to the appropriate schematic.

A8 Front Panel Board Schematic 16

The A8 Front Panel Board circuitry is composed of four functional sections: 1) the seven-segment LEDs in the readout display 2) the discrete LED indicators 3) the switches and 4) the control knob rotary encoder.

The seven-segment LEDs in the readout display are multiplexed by U20 on the A1 CPU Board.

The discrete LED indicators are multiplexed by U22 on the A1 CPU Board.

The switches are scanned by U21 on the A1 CPU Board.

A7 Interconnect Board Schematic 17

The A7 Interconnect Board provides for communication between the A1 CPU Board and the A2/A3 DDS/VCO Boards and the A4/A5 RF Deck and Amp Boards. There are no components mounted on this board.

The SG 5050 signal generation and calibration are controlled by signals from the A1 CPU Board. This board communicates over an asynchronous serial communication link over the A7 Interconnect Board to the A2/A3 DDS and VCO Boards. On this board, these signals are decoded and used in local control loops to control frequency, amplitude and signal routing. The A2/A3 DDS and VCO Boards communicate with its peripheral hardware, and the A4/A5 RF Deck and Amp Boards with a synchronous SPI bus.

Plus and minus 15V power for the A4/A5 and A6 modules are generated on the A2/A3 assembly and transmitted over the Interface Board.

A1 CPU Board Schematics 1,2,3,4

The A1 CPU Board provides the intelligence for instrument control. It processes the various inputs from the front panel and the GPIB, and outputs information back to the front panel. The A1 CPU calculates and transmits all required frequency and amplitude control and calibration constants.

CPU Schematic 1

The CPU consists of U10 and U11. U10 is a 68306 16-bit microprocessor that performs all of the compute intensive tasks required to run the SG 5050. U11 is a PLD device that controls start up, reset, shutdown and the interrupt handling of the CPU. It controls status lights DS2 through DS4.

Also on schematic 1 are the RAM (U6 through U9) and EEPROM (U16 and U19) memories. The RAM is used to store program and operational values during instrument operation. The EEPROM is used to store all the calibration constants necessary for the SG 5050 to produce precision leveled sine wave outputs. The EEPROM is only written to for calibration updates to the SG 5050.

GPIB, NVRAM, Encoder Schematic 2

The NVRAM (U13 and U14) is used to store instrument state information and setup data when power is lost. This would include front panel and/or GPIB status.

The GPIB interface and signal generation are controlled by a special purpose processor U1. This chip communicates with the CPU and generates and decodes all GPIB commands and data. Its output signals go through P1 to the GPIB Board that contains signal buffers and drivers (schematics).

The front panel encoder interfaces to U15 and U17. U15 receives the two phase encoder position pulses and converts then to 8-bit data signals for the CPU. U17 responds to processor control signals to the encoder.

Front Panel Interface Schematic 3

The front panel interface function is performed by U20 through U23. U22 and U23 handle the control panel button inputs and generate indicator outputs. U23 monitors the control panel for operator inputs and generates processor interrupts whenever new data is available. The CPU

then inputs data from U22 to determine which inputs have been selected.

The processor write output display data to U20 and U21 for control of the frequency and amplitude seven-segment displays.

For all other indicator lamp functions, data is written to U22.

A2 DDS/HC11 Controller
Schematics 6,7,8,9

The A2 DDS/HC11 Board provides the intelligence for the precision control of frequency and amplitude. It processes the command inputs form the CPU and generates control outputs to the DDS/VCO and the output Amp/Deck Boards and leveling head. This board also contains the DDS circuitry and its associated frequency reference and output amplifier.

HC11 Controller Schematic 6

The HC11 microcontroller (U1) contains all onboard RAM and ROM necessary for control of the frequency and amplitude loops of the SG 5050. It communicates with the CPU via Q3 and U7 that form an asynchronous serial data link. It receives amplitude and frequency commands and calibration constant data from the CPU, and then sets up all instrument variables to satisfy these commands.

It communicates with the rest of the instrument via J4 pins 18 through 24 that form an SPI-type synchronous serial data link.

On output ports B and C, it generates direct control signals for the DDS and VCO controls. Port A monitors the two PLL lock lines for the reference and VCO phase lock signals. Port A also generates the chip select signals for the SPI interfaces on the RF Deck Board. These signals exit the DDS Board on J18 through J4 and are routed to the RF deck via the A7 Interconnect Board.

DDS/Ref PLL/Output Amp
Schematic 7

This multifunction board performs all of the LF frequency generation and amplitude amplification and control. In addition, it also provides the variable reference frequency to the PLL on the VCO Board.

DDS Reference Schematic 7

The reference frequency for the DDS is generated by the PLL consisting of U12 and U13. This loop is programmed once at SG 5050 start up, and then independently generates the 107MHz clock reference for the DDS. The precision reference oscillator U15 is normally used as the frequency reference for this PLL, however, if an external reference is connected to J7, it is automatically detected by the voltage generated by D6 across C72 and fed to the HC11 controller. The controller then switches K1, a solid state SO relay, to connect the external reference to the PLL. ECL circuit U10 serves to square the input sine wave to a square wave if necessary.

DDS Schematic 7

The DDS consists of U14 and output filters FL1 and FL2. The DDS receives program data from the HC11 uController and converts this data to a current output waveform that is a sine wave at the programmed frequency. The two low pass filters remove any high frequency clock noise from this waveform and produce a low level AC signal that is then amplified to produce the SG 5050 LF output, or is sent to the VCO to be the PLL variable reference input.

Variable Gain Amplifier Schematic 7

U19 through U21 comprise the variable gain amplifier. U19 is the main voltage-controlled variable gain amplifier. This amplifier provides a control range of approximately 40dB. Its gain is adjusted by the variable voltage generated by DAC U16 and op-amps U17 and U18. This voltage ranges from –2.5V to 0V.

Amplifiers U20 and U21 are current mode amplifiers that provide additional gain and drive capability. They amplify the signal to a level of approximately +28dBm at maximum output of the SG 5050. At the output of U21, there are two selectable low pass filters to remove unwanted harmonics from the output. FL3 has a 15MHz corner frequency, and FL4 has a 30MHz corner frequency. At 15MHz and above, the output is switched to FL4; below that frequency FL3 is used. Relay K2 is used to switch the output of the DDS to either the VCO or the output amp and attenuator assembly.

A3 VCO Board Schematics 10,11,12

The A3 VCO Board provides the frequency generation capability of the SG 5050 over the HF band from 25.000001MHz to 2500.000MHz.

PLL and Loop Filter Schematic 11

The PLL chip (U13) serves as the primary frequency control element for the HF band. Refer to the Circuit Theory Notes at the start of this chapter for basic PLL operations.

Digital programming information is sent to the PLL over the SPI interface on J3-9, 10 and 15. This data programs the internal dividers that determine output frequency. The reference signal on J2 is also used for fine resolution of the output frequency and varies in the 9.8 to 11.8MHz range. U14 is an ECL logic device that is used an as input squaring circuit to convert the reference sine wave to a square wave and to effect AC coupling of the reference input.

A sample of the VCO output frequency is routed to the PLL phase detector input and is labeled F_FEEDBACK.

The PLL output is in the form of narrow pulses on pins 36 and 37. These pulses are integrated and low pass filtered by U16. The corner frequency of this filter is approximately 500Hz. L1, C51, C52 and C55 form a notch filter to remove any of the reference frequency that might leak through the phase detector outputs. The DC voltage produced at the output is called VTUNE and is used to control the VCO output frequency. Currently, U15 and its associated circuitry are not populated, and this circuit is bypassed via jumpers on the PC board.

VCO and Switch Matrix Schematics 10,11

There are seven different VCOs that are used to generate the output frequencies of the SG 5050. They cover the output frequency range in the following order:

U12	25MHz to 50MHz
U11	50MHz to 100MHz
U9	100MHz to 200MHz
U8	200MHz to 400MHz
U6	400MHz to 800MHz
U4	800MHz to 1350MHz
U3	1350MHz to 2500MHz

Only one VCO is selected at any given time. This selection is controlled by U10 and the SPI interface on (schematic 11). They generate the signals ENA1* through ENA7*. These signals are used to turn on

the power and to switch the VCO outputs to the output transmission line.

Take as an example U12 the 25 to 50MHz VCO. When it is to be selected, ENA1* goes low while all other ENA signals remain high. This turns on the P-channel FET Q7 allowing power to be applied to U12. This also controls the solid state RF switch K3 and allows RF to pass from pin 5 to pin 8. Since only one VCO is powered at any one time, this eliminates any interference problems and allows VTUNE to be routed to all VCOs without any switching. The VCO outputs are all tied to the same RF transmission line that goes to the power splitter comprised of R22, R23 and R25. This power splitter evenly divides power between the output J1 and the PLL. It also serves to isolate the VCO output, the PLL input and the amp and filter input from each other.

Two of the VCOs have lower VTUNE maximum voltage specifications than the others. The VTUNE inputs to these VCOs (U11 and U12) are protected by clamp diodes D1 and D2 that are driven by U17 and U18. The clamps are set at 14.5V. When the VTUNE signal to these two VCOs goes over this value, the diodes conduct and the VTUNE voltage is dropped across R36 and R38 to a safe level.

A4,5 RF Amplifier and Deck Schematics 13,14

The A4,5 RF Amplifier and Deck are a piggyback board assembly that provides for signal amplitude control of the SG 5050 output. The A4 deck assembly consists of the control and measuring circuitry and the A5 amplifier consists of the RF processing and amplification circuitry.

SPI Interface Schematic 13

The SPI interface consists of U5, U6, U7, U8 and U15. These chips receive the SPI signals on J6-19, 20 and 22 and decode all necessary signals to control the filters, amplifiers and attenuators on the A5 amplifier assembly.

Filter Tune Schematic 13

The tuning voltages for the variable low pass filters are generated by U12 and U17. U12 is a D/A converter that converts serial SPI bus programming to two dual 0-23V DC levels that are used to control filter cutoff frequencies.

Attenuator Control Schematic 13

D/A converter U11 and op-amp U16 generate the control voltages for the 0-40dB attenuator on the A5 Amplifier Board. The circuit generates two voltages that vary between –1.8V to –2.3V to control the amount of attenuation at the filter inputs. Transistor Q2 allows for programming a second range of –2.3V to –2.8V. The two voltages generated are output at J4-13 and 14 and are complementary. For example, the voltage at J4-14 will move from –2.3V to –1.8V, and the voltage at J4-13 will move from –1.8V to –2.3V at the same time.

A/D Converter and Amplitude Detection Schematic 13

The measurement of the output amplitude to allow leveling of the SG 5050 output is performed by U13, U10, U14 and U16. The RF signal is detected in two different places depending on the frequency. From 10KHz to 1MHz the amplitude is detected by the precision rectifier composed of U10 and D5. This signal is digitized by U13 and read by the HC11 uProcessor to

generate amplitude programming levels to control the variable gain amplifier (VGA) on the A2 DDS Board.

From 1MHz to 2500MHz the leveling head detects the signal amplitude at the OUTPUT and converts this to a DC level that is input at J1-4. This level is buffered by U16, read by U13 A/D converter and sent to the HC11 uProcessor to generate programming levels for the VGA from 1MHz to 25MHz, and then to control the VVA from 25MHz to 2500MHz. Since the input at J1-4 might vary from 0 to 8V, and the A/D converter only has a 0 to 5V range, Q3, R60 and U11 provide a variable input offset and gain to increase the range of the A/D converter. With Q3 enabled and U11 set to OV, the gain of the amplifier U16 increases by five. With Q3 disabled and U11 set to +4V, the AD converter can digitize signals from +4V to +9V. The HC11 uProcessor then performs the required task to normalize the signal values.

In addition to the two level detection signals, the A/D converter also monitors a signal called HD_TEMP on J1-5. This signal is used to determine that the head is properly connected and is operating within its normal temperature range.

U16, U17 and D2, D3 and D4 protect the input to the A/D converter from seeing fault conditions of voltages below 0V and above 5V. They are precision clamps that do not allow the A/D converter inputs to exceed these values.

Voltage Tuned Filter/Attenuator
Schematic 14

The output of the A3 VCO has significant levels of 2nd, 3rd and 4th harmonic of the fundamental frequency. In order to remove these harmonics to meet SG 5050 output specifications, a voltage tuned low-pass filter is inserted in the signal path between the VVA U1 and the output amplifiers and attenuator that start at K1.

This filter is constructed in three bands, VHF (enabled by Q1 and Q13), UHF_LO (enabled by Q2 and Q12) and UHF_HI (enabled by Q3 and Q9). Each filter works in a similar manner and are tuned by a variable voltage (VTUNEs 1 and 2) that control the capacitance of varactor diodes D1 through D10. In addition to the major bands, the two lowest frequency filters are broken into subbands. The VHF filter has three bands and the UHF_LO filter has two bands. The filter bands are as follows:

VHF Band 0	25MHz to 55MHz
VHF Band 2	55MHz to 125MHz
VHF Band 1	125MHz to 230MHz
UHF_LO Band 0	230MHz to 550MHz
UHF_LO Band 1	550MHz to 1000MHz
UHF_HI	1000MHz to 2500MHz

The filters and bands are enabled by Q1 through Q13. These FETs turn on at 0V and are cut off by –5V.

The main amplitude control for the SG 5050 is performed via U1, the VVA. This attenuator has a 0 to –40dB range and is used in conjunction with the output attenuators and amplifiers to control the actual output level. The HC11 uProcessor performs the actual control task by selecting attenuation and amplifier settings to produce the proper output at the leveling head. The HC11 uProcessor is programmed by the main CPU as to what the proper output voltage from the head should be for any frequency/amplitude combination. The main CPU performs calculations based on the known response curve of the leveling head (stored calibration data), and the requested output amplitude and frequency are then

downloaded to the HC11 as a "control to" voltage level. The HC11 then sets all required outputs and completes the control loop as necessary to maintain the output at the proper level.

Output Amplifiers/Attenuators
Schematic 14

At the input to the amplifiers and attenuators, K1 selects between the LF or HF band inputs. In the LF band, a variable amplitude signal is fed from the A2 board and two 20dB fixed attenuators (K2 and K3) are used to produce the lowest (-43dBm) output levels. The signal is also routed around the HF amplifier section by K4 and K5 (shown in their NC position). Transistor Q15 is selfbiased on by R45 and R51, and reverse biased diode D18, pin J5-8 is set to +24V. This output appears at J3 for routing to the leveling head. The level at J3 will vary from approximately +28dBm to –37dBm.

When the HF band is selected, the HC11 uProcessor selects the proper combination of amplifiers and attenuators in order to produce the programmed level. In order to maintain a low noise level in the output, the amplifiers are turned on in stages. U3 and U4 come on first, then U2. The exact switch points of amplifiers are frequency dependent and are controlled by calibration constants stored in the CPU. The basic sequence is as follows:

Programmed Output	Amp/ Attenuator
-43 to ≈ -20dBm	no amp/pass through
-20 to ≈ -10dBm	U3, U4 and attenuator K6
-10 to ≈ +10dBm	U3, U4
≈+10 to +18.75dBm	U2, U3, U4

The amplifiers are all class A linear amplifiers and are implemented as hybrid chips. Attenuator K6 is a 10dB attenuator formed out of discrete components on the Amplifier Board. All signal paths are designed using microstripline techniques to maintain a constant 50Ω impedance, and all devices are matched to 50Ω to maintain a low VSWR.

A6 Leveling Head Schematic 15

The A6 Leveling Head provides for the precise control of the output amplitude to provide leveled sine waves at the DUT input. It consists of a precision power splitter (R16, R17 and R18) that divides the input power between the measurement circuit and the output. This divider also provides for the precise 50Ω output impedance.

The signal level is controlled at the input to the detector to remain in a –43dBm to –27dBm range by the two-bit attenuator (U1). This provides for 0, 16, 32 or 48 dB attenuation levels. The reason for controlling the signal level to this range is to allow the detector diode (D1) to operate in the –11 to +5dBm range. In this range the diode output is relatively linear with power and provides for detectable signals without large amounts of DC signal gain.

Low level signals at the input are amplified by U2, U3 and U4. Each amplifier has a nominal 12dB gain for an overall gain of +36dB.

The detector diode (D1) is a matched pair in a single SOT-123 package. This allows for very close performance matching and temperature compensation. The diodes are both biased at approximately 15 microamps. This increases their sensitivity and allows nulling of any temperature effects by only looking at the differential output voltage at U5 pins 2 and 3. Additionally, the temperature compensation voltage is output at U5-16 to detect any head problems or disconnects. This voltage is nominally +4.0V at 25° Celsius and decreases with increasing temperature.

The output of the leveling head is not linear with respect to amplitude and is not constant over frequency. Therefore, both frequency and level calibrations are performed and calibration constants along with math routines to linearize the response are stored in the SG 5050 CPU. For this reason calibration must be performed with the leveling head that is to be used with the SG 5050, and if that head is damaged, calibration must be reperformed with a new or repaired head.

Warning

The following servicing instructions are for use only by qualified personnel. To avoid personnel injury, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so. Refer to General Safety Summary and Service Safety Summary prior to performing any service.

SECTION 5
PERFORMANCE CHECK

INTRODUCTION

This procedure checks the electrical performance requirements as listed in the Specifications section of this manual and may be used in an incoming inspection facility to determine acceptability of performance. If the instrument tails to meet the requirements given in this Performance Check section, the Adjustment Procedure section should be performed. The Performance Check procedure can be performed at any ambient temperature between 0° and +40° Celsius.

Performance Check Interval

The performance check should be performed at the following intervals:

- At incoming inspection.
- After 2000 hours of operation or every twelve months, if used infrequently.
- After repair of accidental abuse.

Services Available

TEGAM, Inc. provides complete instrument repair facilities at local field service centers and at the factory service center. Contact your local TEGAM field office or representative for more information.

Conventions Used in this Procedure

All reference to the SG 5050 front panel controls, connectors and indicators will be indicated by all capital letters. All associated equipment front panel controls, connectors and indicators will be indicated by initial capital letters.

TEST EQUIPMENT REQUIRED

The test equipment, or equivalent (except as noted), listed in Table 5-1 is recommended to perform the Performance Check and Adjustment Procedure in this manual.

Table 5-1: Required Test Equipment

Description	Minimum Requirement	Performance Check	Adjustment Procedure	Recommended Equipment
TM 5000Sseries Power Module	Compatible with SG 5050.	X	X	Tektronix TM 5006A
Digital Counter	Timebase accurate to 0.75PPM into 50Ω load.	X	X	Hewlett Packard HP 5350B
GPIB Controller	IBM PC and GPIB adapter card.		X	
Digital Voltmeter	0.25% AC accuracy, 1Hz to 100KHz, 55mV to 5.5V.	X	X	Hewlett Packard HP 3458A Multimeter
Spectrum Analyzer	Frequency range 10KHz to 10GHz, resolution bandwidth 1KHz to 3MHz, reference level range – 50dBm to +20dBm, frequency response flatness to 10GHz <±3.0dB.	X	X	Hewlett Packard HP8593E Prog. Spectrum Analyzer
Power Meter	Frequency range 10MHz to 3GHz, power range – 70dBm to +20dBm.	X		Boonton
Power Sensor	Frequency range 10MHz to 3GHz, power range – 70dBm to +20dBm. Calibrated at test frequencies.	X		Boonton
Precision 50Ω SMA feedthrough Termination	50Ω ±190DC, 1/2W, VSWR <1.06 to 10MHz.	X	X	
Adapter	SMA female to dual banana plug.	X	X	
Adapter	SMA female to N female	X	X	
Adapter	SMA female to N male.	X	X	
Coaxial 50Ω cable (two required)	BNC male to BNC male, 36".	X	X	Tektronix part 012-0057-01

PREPARATION

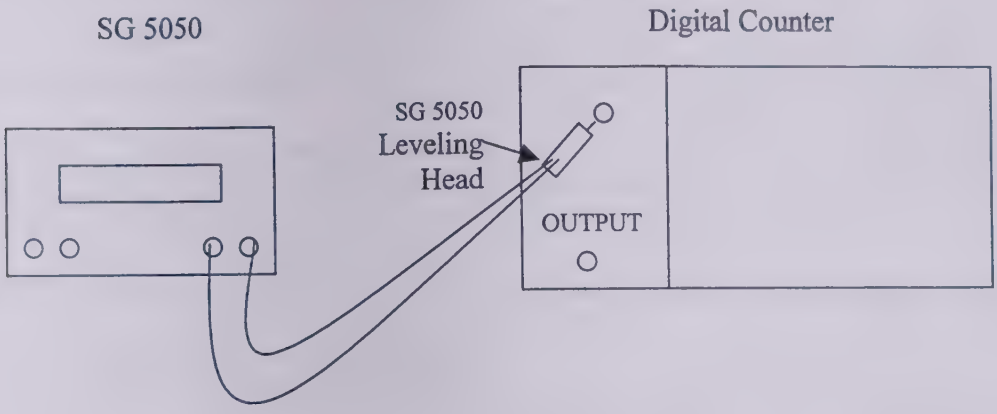
a. Insert the SG 5050 into the power module. Connect the test equipment and the power module to a suitable line voltage source.
b. Turn on the power module and test equipment, and allow at least thirty minutes warm-up.

Check Frequency Accuracy

This test verifies the output frequency accuracy (10KHz through 2.5GHz).

a. Setup the equipment as illustrated in Figure 5-1.

REFER TO TABLE 5-1, TEST EQUIPMENT REQUIRED



SG 5050

AMPL button.....Selected
DATA keypad.....5.5V
FREQUENCY VARIABLE button.....Selected
DATA keypad.....10KHz
OUTPUT HEAD ON/OFF.....ON

FIGURE 5-1: Frequency Accuracy Check

b. Check digital counter readout is 10KHz, within the limits of 9.939970KHz to 10.06003KHz.

c. Enter 14.9999KHz on the SG 5050 data keypad.

d. Check digital counter readout is 14.9999KHz, within the limits of 14.999825KHz to 14.999975KHz.

e. Enter 15.0000KHz on data keypad.

f. Check digital counter readout is 15KHz, within the limits of 14.999685KHz to 15.000315KHz.

g. Enter 49.999KHz on data keypad.

h. Check digital counter readout is 49.999KHz, within the limits of 49.99855KHz to 49.99945KHz.

i. Select frequency reference button (50KHz).

j. Check digital counter readout is 50KHz, within the limits of 49.99685KHz to 50.00315KHz.

k. Select frequency variable button.

l. Enter 10MHz on data keypad.

m. Check digital counter readout is 10MHz, within the limits of 9.999967MHz to 10.000033MHz.

n. Enter 10.00001MHz on data keypad.

o. Check digital counter readout is 10.00001MHz, within the limits of 9.999977MHz to 10.000043MHz.

p. Enter 550MHz on the data keypad.

q. Check digital counter readout is 550MHz, within the limits of 549.998347 to 550.001653MHz.

r. Enter 1000MHz on the data keypad.

s. Check digital counter readout is 1000MHz within the limits of 999.997MHz to 1000.003MHz.

t. Enter 2500MHz on the data keypad.

u. Check digital counter readout is 2500MHz within the limits of 2499.998MHz to 2500.008MHz.

Check Spectral Purity

This test verifies that the amplitude of the 2nd harmonic is less than –30dBc, the amplitude of the 3rd is less than –35dBc, and higher harmonics (only tested through 5th harmonic) are less than –40dBc of the fundamental frequency. The test is made at the SG 5050's maximum amplitude, which is the condition for worst case harmonics.

The test starts with a spot check below 50KHz and then sweeps the SG 5050 frequency using the front panel control knob up to the maximum frequency. The operator should adjust the spectrum analyzer to maintain at least five harmonics on the screen at all times. The operator will have to continuously adjust start and stop frequencies and band selections in order to perform measurements.

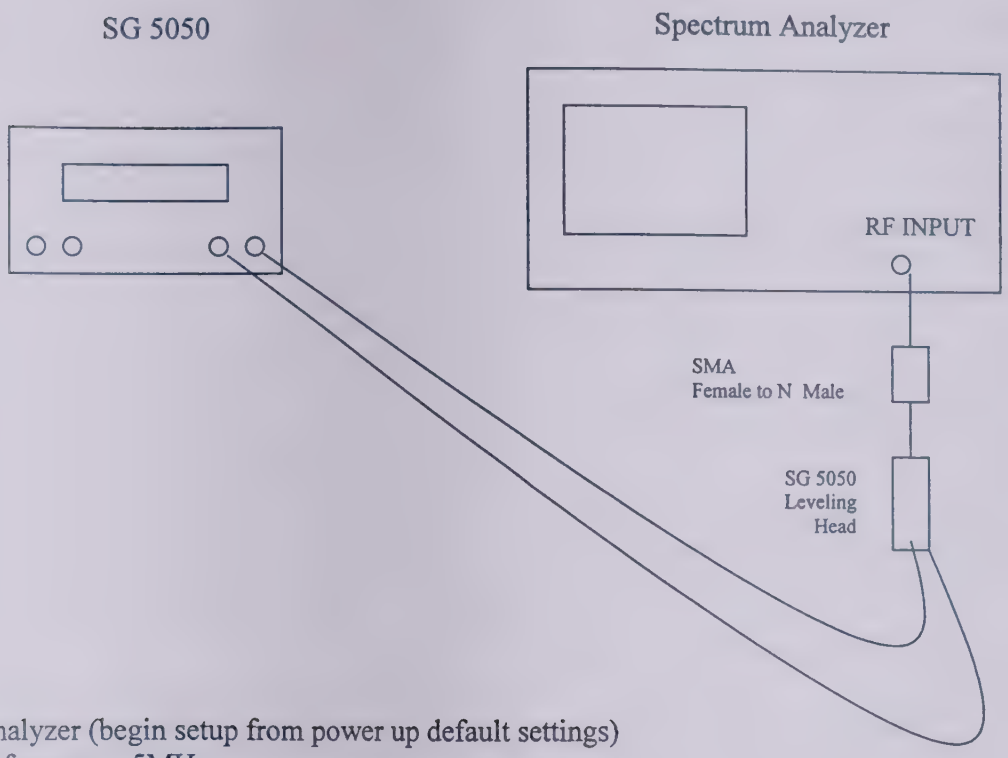
a. Setup the equipment as illustrated in Figure 5-2.

b. Find the first peak. This should set the marker on the peak of the 10MHz signal.

c. Set the ref level on the spectrum analyzer to +20dBm ±1dBm. The ref level should not be changed during the rest of the procedure.

d. Set SG 5050 frequency to 50KHz. Set the spectrum analyzer start/stop frequencies to 20KHz and 300KHz respectively.

REFER TO TABLE 5-1, TEST EQUIPMENT REQUIRED



SETUP

Spectrum Analyzer (begin setup from power up default settings)

- Start frequency 5MHz
- Stop frequency 50MHz
- Amplifier ref +20dBm
- Marker on
- B.W. 100KHz

SG 5050

AMPL button	Selected
DATA keypad	5.5V
FREQUENCY VARIABLE button	Selected
DATA keypad	10MHz
OUTPUT HEAD ON/OFF	ON

FIGURE 5-2: Spectral Purity Check

e. Check the 2nd harmonic amplitude peak is at least 3 divisions (-30dBc) and that the 3rd harmonic amplitude peak is at least 3.5 divisions (-35dBc) below the top horizontal graticule line (fundamental reference amplitude).

f. Check that 4th and 5th harmonic amplitude peaks are at least 4 divisions (-40dBc) below the top horizontal graticule line.

g. Use the digit select buttons on the SG 5050 to set the control knob resolution to 10KHz. Then using the control knob, slowly increase the SG 5050 frequency to 1MHz. While increasing the SG 5050 frequency to 1MHz, monitor the harmonics using the spectrum analyzer as in steps e and f.

NOTE

In this and all of the following steps, as the SG 5050 frequency is increased the spectrum analyzer center frequency and span will need o be increased to allow the first five harmonics of the SG 5050 output frequency to be observed. Be careful that the spectrum analyzer span is not made too large compared to the frequency being measured or the accuracy of the amplitude measurement may be compromised.

h. Use the digit select buttons to set the control knob resolution to 100KHz. Then using the control knob, increase the SG 5050 frequency to 10MHz. While increasing the SG 5050 frequency to 10MHz, monitor the harmonics using the spectrum analyzer as in steps e and f.

i. Use the digit select buttons to set the control knob resolution to 1MHz. Then using the control knob, increase the SG 5050 frequency to 25MHz. While increasing the SG 5050 frequency to 25MHz, monitor the harmonics using the spectrum analyzer as in steps e and f.

j. Set control knob resolution to 10MHz.

k. Use the SG 5050 control knob to increase the frequency to 2500MH. While increasing the SG 5050 frequency to 2500MHz, monitor the harmonics using the spectrum analyzer as in steps e and f.

Check Amplitude Accuracy

A worksheet (Table 5-2) is provided at the end of this check to record the various measurement readings required. These measurement readings will be used to calculate the accuracy of your instrument.

This test verifies amplitude accuracy from 10KHz to 50KHz.

a. Setup the equipment as illustrated in Figure 5-3. The DVM is configured to measure AC RMS volts using synchronous sampling conversion.

b. Check DVM readout for 19.445mV AC, within the limits of 19.154 to 19.737mV.

c. Record the DVM readout on line 1 column 1 in Table 5-2 Part 1 (located in step 4) for 50KHz data.

d. Enter 500mV on the SG 5050 data keypad.

e. Check DVM readout for 0.19445V AC, within the limits of 0.19154V to 0.19737V.

f. Record the DVM readout on line 2 column 1 in Table 5-2 Part 1 (located in step 4).

g. Enter 552mV on the SG 5050 data keypad.

h. Check DVM readout for 0.19516V AC, within the limits of 0.19223V to 0.19809V.

i. Record the DVM readout on line 3 column 1 in Table 5-2 Part 1 (located in step 4).

j. Enter 1V on the SG 5050 data keypad.

k. Check DVM readout for 0.35355V AC, within the limits of 0.34825V to 0.35886V.

l. Enter 2.5V on the SG 5050 data keypad.

m. Check DVM readout for 0.88388V AC, within the limits of 0.87062V to 0.89714V.

n. Enter 5.5V on the SG 5050 data keypad.

o. Check DVM readout for 1.9445V AC, within the limits of 1.9154V to 1.9737V.

p. Record the DVM readout on line 4 column 1 in Table 5-2 Part 1 (located in step 4).

q. Select the SG 5050 frequency variable button and enter 10KHz on the data keypad.

r. Select SG 5050 ampl button and enter 552mV on the data keypad.

s. Check DVM readout is 0.19516V AC, within the limits of 0.19223V to 0.19809V.

t. Enter 5.5V on the SG 5050 data keypad.

u. Check DVM readout is 1.9455V AC, within the limits of 1.9154V to 1.9737V.

v. Select the SG 5050 frequency variable button and enter 10MHz on the data keypad.

w. Check DVM readout is 0.19516V AC, within the limits of 0.19223V to 0.19809V.

x. Select the SG 5050 ampl button and enter 5.5V on the data keypad.

y. Check DVM readout is 1.9445V AC, within the limits of 1.9154V to 1.9737V.

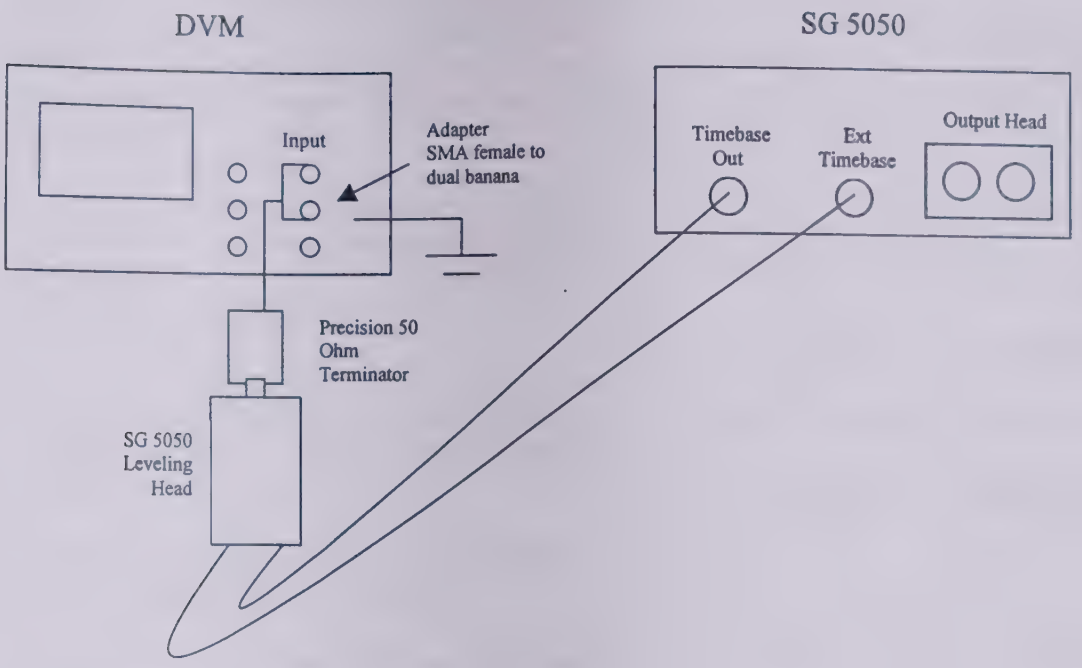
z. Select the frequency variable button and enter 49.999KHz on the data keypad.

aa. Check DVM readout is 1.9445V AC, within the limits of 1.9154V to 1.9737V.

bb. Select the ampl button and enter 552mV on the data keypad.

cc. Check DVM readout is 0.19516V AC, within the limits of 0.19223V to 0.19809V.

REFER TO TABLE 5-1, TEST EQUIPMENT REQUIRED



SETUP

Digital Voltmeter

Blue button	Press
Reset button	Press
ACV button	Select
Blue button	Press
S	Press
Down arrow	Press until SETACV
Right arrow	Press once
Down arrow	Press until SETACV SYNC
Enter button	Press

SG 5050

FREQUENCY REFERENCE button	Selected
AMPL button	Selected
DATA keypad	55mV
OUTPUT HEAD ON/OFF	ON

FIGURE 5-3: Amplitude Accuracy Check

Check Amplitude Flatness

This test verifies amplitude flatness from 10MHz to 2500MHz. SG 5050 flatness is checked with a combination of procedures. Frequencies below 10MHz are check with a DMM. Then a power meter is used to compare the 10MHz accuracy out to 2500MHz.

a. Setup the equipment as illustrated in Figure 5-3. The DMV is setup to measure AC RMS volts with the frequency variable adjusted for the frequency being tested.

b. For each amplitude set, measure the output level at 10KHz, 50KHz, 100KHz, 1MHz, 5MHz and 10MHz. Accuracy must be setting ±1.5%.

c. Set and measure as in step b above –28dBm, -12dBm, +4dBm and +18.75dBm.

d. Convert to volts p-p and compare with settings. Answers must be correct within ±1.5%.

e. Connect SG 5050 to power meter. Set output frequency to 10MHz. Read and record values at -28dBm, -12dBm, +4dBm and +18.75dBm.

f. At each of the following frequencies, read the output of the SG 5050 at the levels given in step e above and compare against the specified limits.

g. Set to 100MHz. Compare levels ±1.5%.

h. Set to 250MHz. Compare levels ±3.0%.

i. Set to 500MHz. Compare levels ±4.0%.

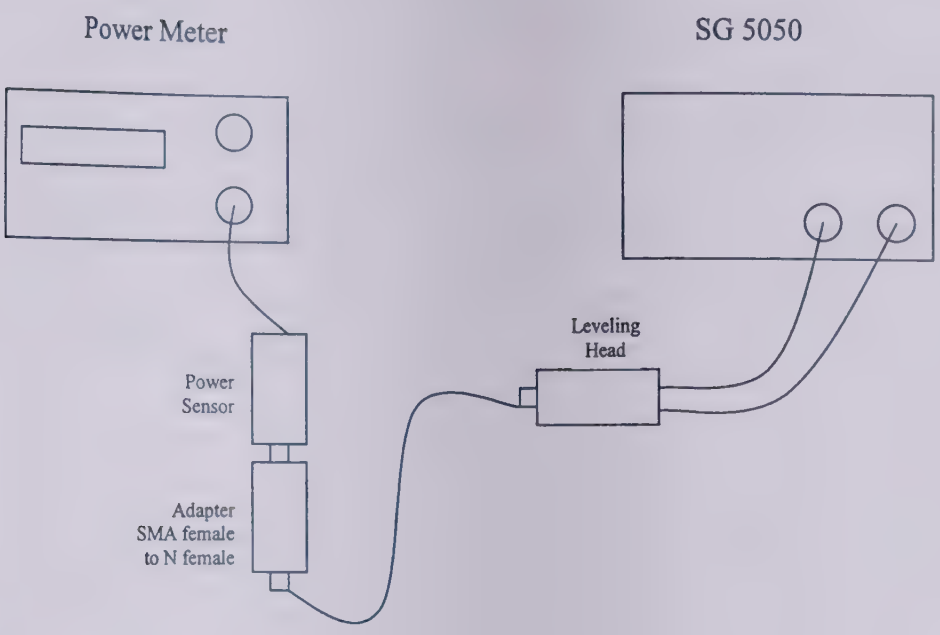
j. Set to 1000MHz. Compare levels ±4.0%.

k. Set to 2500MHz. Compare levels ±4.0%.

NOTE

Be sure to always enter power meter's frequency correction factor correctly.

REFER TO TABLE 5-1, TEST EQUIPMENT REQUIRED



SETUP

Power Meter – set to measure dBm at the frequency of interest

SG 5050

FREQUENCY VARIABLE button.....Selected
DATA keypad.....10MHz
AMPL button.....Selected
DATA keypad.....55mV
OUTPUT HEAD ON/OFF.....ON

FIGURE 5-4: Part 2 Amplitude Flatness Check

Table 5-2: Amplitude Flatness Worksheet

(50 kHz to 100 kHz)

Line No.	SG 5030		Column 1	Column 2	Ratio Limits	
	Frequency	Amplitude	DVM Reading	DVM Amplitude Ratio	Lower Limit	Upper Limit
1	50kHz	55mV				
2		550mV				
3		552mV				
4		5.5V				
5	75kHz	55mV			0.985	1.015
6		550mV			0.985	1.015
7		552mV			0.985	1.015
8		5.5V			0.985	1.015
9	100kHz	55mV			0.985	1.015
10		550mV			0.985	1.015
11		552mV			0.985	1.015
12		5.5V			0.985	1.015

SECTION 6
ADJUSTMENT PROCEDURE

INTRODUCTION

The calibration procedure for the SG 5050 is performed by the TEGAM software running on the equipment setup listed in Table 5-1. It automatically controls the instruments and informs the operator when to change connections or change instrument setup. All data is recorded internally and used by the instrument controller to develop the calibration data tables that are loaded into the instrument's NVRAM. At the completion of the calibration, an automatic verification program is run and before and after results are generated. It is estimated that this complete procedure should take approximately four hours.

Table 5-1: Required Test Equipment

Description	Minimum Requirement	Perf. Check	Adjustment Procedure	Recommended Equipment
TM5000 Series power module	Compatible with SG 5050	X	X	TM-5006A
Digital Counter	Time base accurate to .75PPM into 50Ω	X	X	
Spectrum Analyzer	Frequency 9KHz to 26.5GHz Resolution BW 1KHz to 3MHz Reference level range –50dbm to +20dbm Response flatness <±3dbm.	X	X	HP8593E Hewlett Packard
Digital Voltmeter	.25% AC accuracy 10KHz – 10MHz 5.5mV to 5.5V	X	X	HP3458A Hewlett Packard
30MHz Receiver	30MHz ±2MHz Sensitivity –110dbm Accuracy –10 to –100 ±.005dbm/10db	X	X	Weinschel model UM-7
.01 to 18GHz Frequency Converter	See attached	X	X	Weinschel model 8852
Instrument Controller GPIB	IBM PC or equivalent with GPIB interface	X	X	
Control Software	TEGAM XXXX	X	X	No substitution

PREPARATION

a. Adjustments must be performed in an instrument that has had its top cover removed and in a power module with the top cover removed. Refer to manual for cover removal instructions.

b. Using a screwdriver, remove the oscillator adjustment cover on the A2 DDS Board assembly.

c. Connect the test equipment and power module to a suitable line voltage source, turn on and allow to warm for a minimum of thirty minutes.

d. During warm up, connect the SG 5050 leveling head to a suitable 50Ω dummy load, and set for +18dBm output at 1000MHz.

Adjust Output Amp Power Supply

With the SG 5050 set as in 1d above, connect a voltmeter to board A5 J5 pin 1 +lead and a board mounting screw to the –lead. Voltmeter should read 15V ±.1V. Adjust R59 and A4 if necessary.

Adjust Internal Timebase Frequency

a. Connect SG 5050 timebase out to a suitable counter.

b. Prepare as in section 1.

c. Adjust oscillator on A2 DDS Board with an insulated alignment tool to a readout of 10.000000MHz ±.000010 if necessary.

d. Replace adjustment cover when finished.

Adjust Amplifier Power Supply

a. Remove instrument top cover.

b. Connect DVM to amplifier power supply.

c. Insert instrument into extender test fixture.

d. Connect leveling head.

e. Turn instrument on.

f. Set output to 1GHz at 5V.

g. Read voltage and adjust to 15V ±.15V.

h. Power down and disconnect.

PERFORM INSTRUMENT AMPLITUDE CALIBRATION

The amplitude calibration is performed via a computer and automated measuring equipment. All instruments must be connected via the GPIB bus and the specified software installed. The calibration then involves running and following the software instructions. At the end of this process, the control computer will automatically update the calibration data table that is in the SG 5050 CPU.

The operator must setup the equipment according to Figure 6-1 and then start the calibration software. The operator will be instructed for any further actions required by the readout on the computer's CRT.

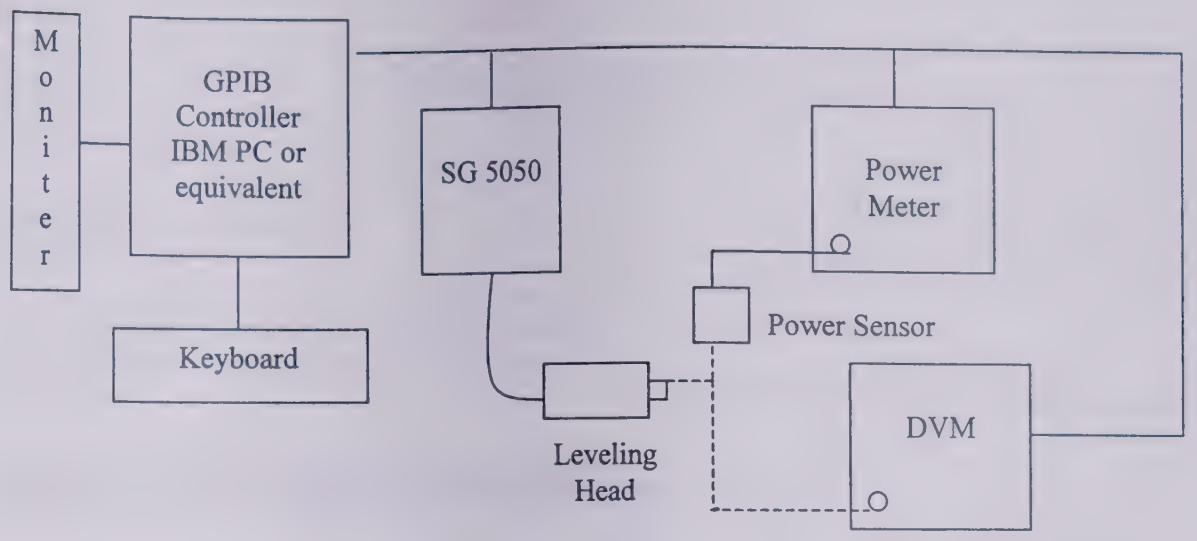


FIGURE 6-1: Instrument Amplitude Calibration

SECTION 7
MAINTENANCE

INTRODUCTION

This section of the manual gives rear interface information and provides general maintenance and service information for the SG 5050 Sine Wave Generator.

CAUTION

To prevent damage to the SG 5050, turn off the power module before installing or removing the instrument. Do not use excessive force to install or remove the SG 5050 from the power module.

Rear Interface Information

The pin assignments shown in Figure 7-1 are identical for the A1 306 uComp Board and the A4-A5 Output Board.

Figure 7-2 shows the pin assignments for the GPIB connector on the A3 CPU Board. Figure 7-3 shows the pin assignments for the A6 Timebase Board.

GENERAL MAINTENANCE

Loss of NVRAM

Stored setups and the current contents of the SG 5050 front panel buffer will be lost upon failure of either one or both of the internal NVRAMs (front panel error codes 363 and 354).

Upon NVRAM failure, either one or both of these NVRAM ICs must be replaced to restore the nonvolatile memory capability. The SG 5050 must be recalibrated and all stored setups must be re-entered upon completion of any NVRAM replacement.

TROUBLESHOOTING AIDS

Diagrams

Complete circuit diagrams are located in the pullout pages in the Diagrams, Schematics and Illustrations section of this manual. The portions of the circuit mounted on the circuit boards are enclosed by a solid line. The circuit number of each component in this instrument is shown on a diagram.

Circuit Board Illustrations

Circuit board illustrations are provided in conjunction with the circuit diagrams. Each board-mounted component shown on a diagram is also identified on the circuit board illustration by circuit number. A lookup table is provided with each diagram, listing components by circuit number.

Transistor and Diode Pinouts

Most active devices in the SG 5050 are shown on the schematics with pin numbers usually referenced to an orientation mark. There is no pin number information on transistors and diodes since they have a standard naming convention for a given case style.

A4 DDS BOARD AND A7 OUTPUT BOARD PLUG-IN REAR VIEW

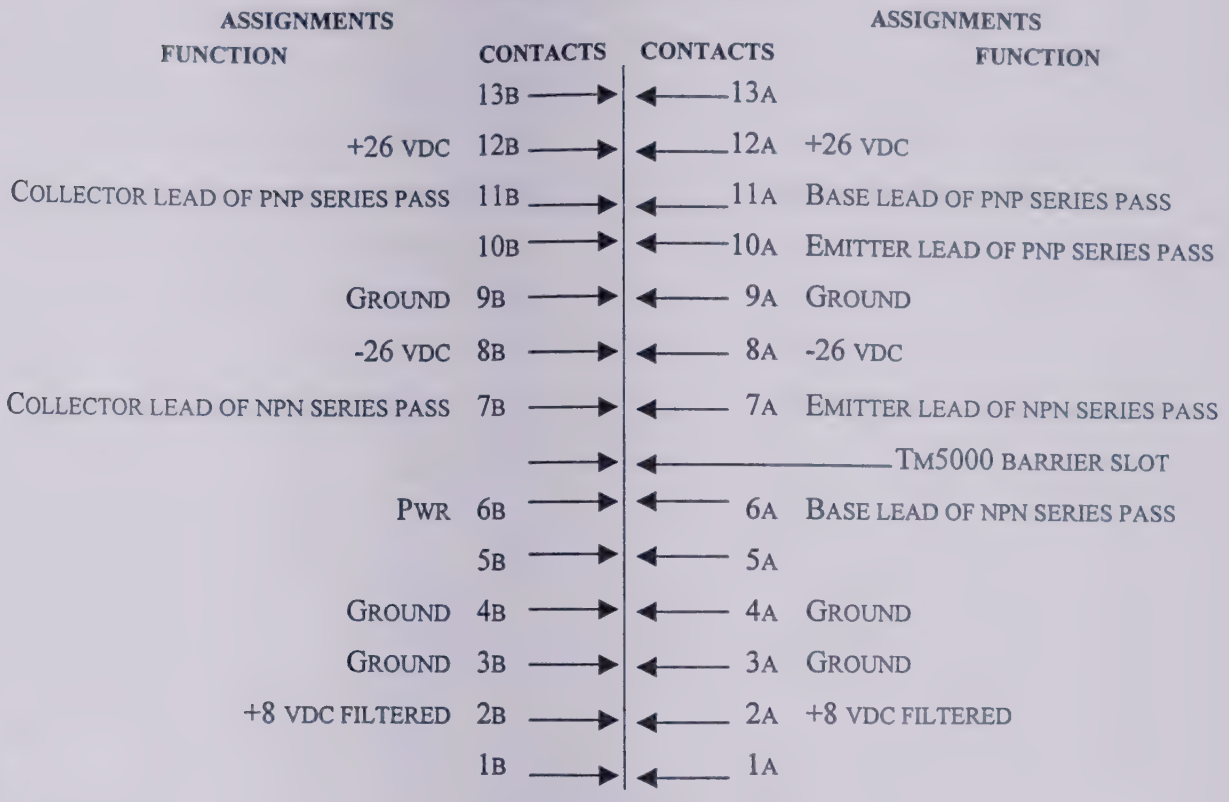


FIGURE 7-1: CPU and Output Board Rear Interface

REAR INTERFACE GPIB CONNECTOR
PLUG-IN REAR VIEW

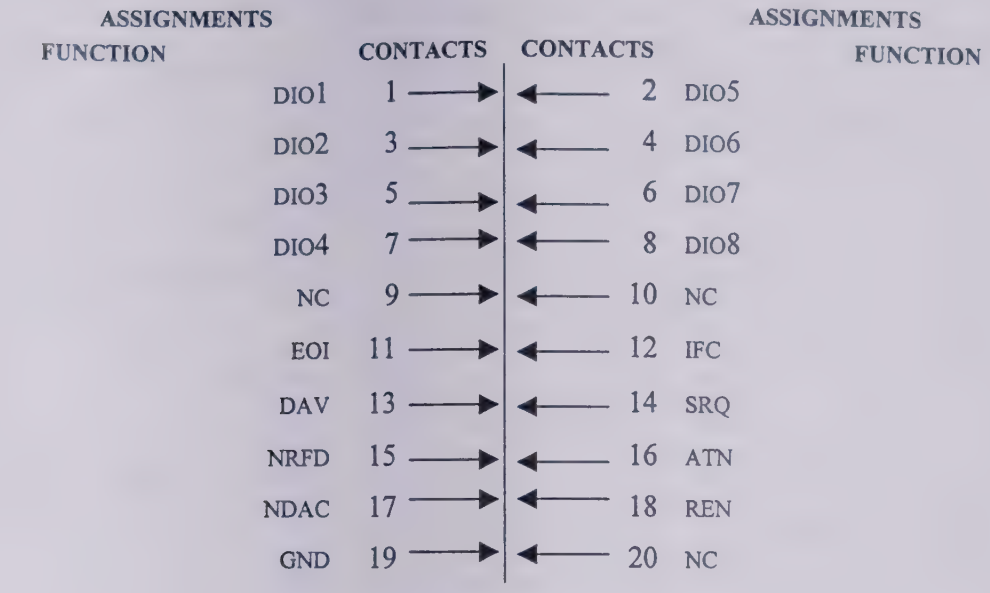
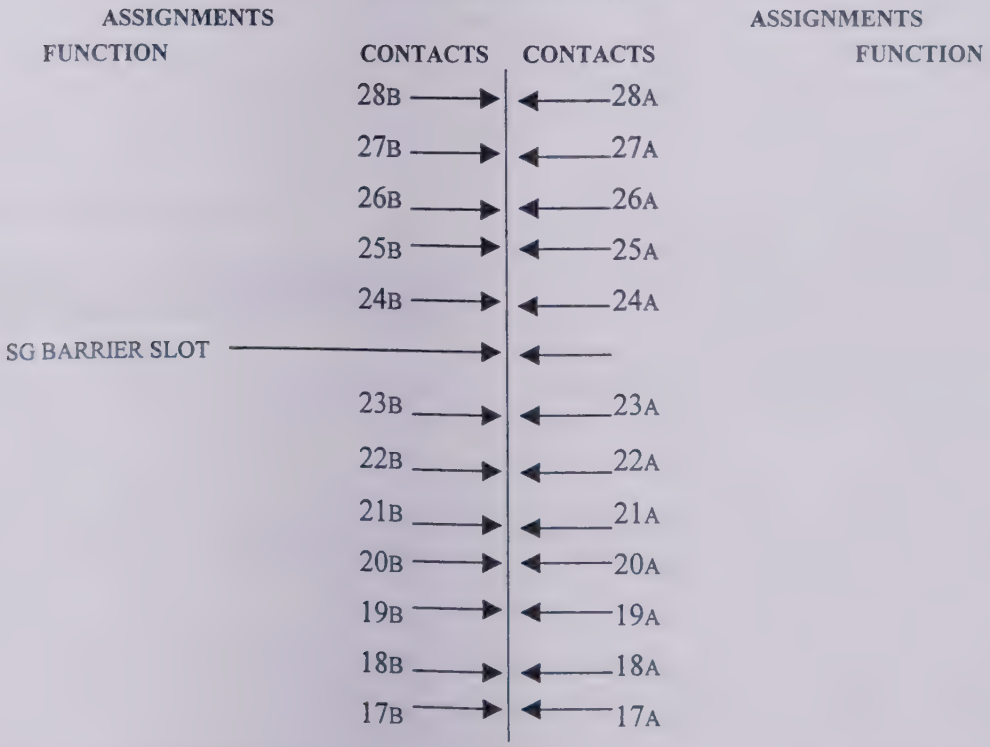


FIGURE 7-2: GPIB Rear Interface

A2-A3 DDS-VCO BOARD
PLUG-IN REAR VIEW



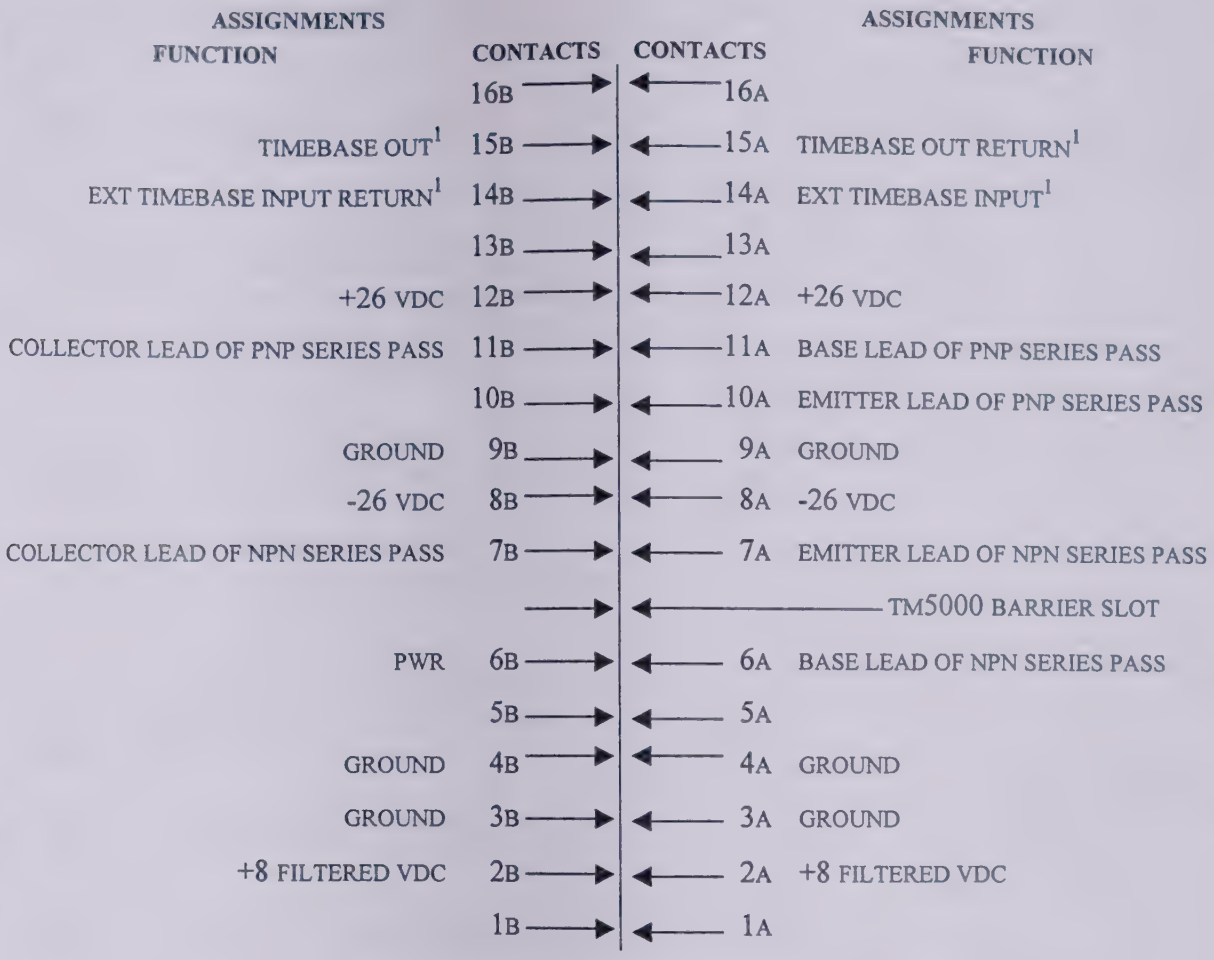


FIGURE 7-3: DDS/VCO Board Rear Interface

Static Sensitive Components

CAUTION

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. See Table 7-1 for relative susceptibility of various classes of semiconductors. Static voltages of 1kV to 30kV are common in unprotected environments.

[1] These rear connector functions are active only when the coaxial cables are removed from the front panel connectors and reconnected to J3050and J3051 on the A6 Timebase Board.

Observe the following precautions to avoid damage:

1. Minimize handling of static-sensitive components.
2. Transport and store static-sensitive components or assemblies in their original containers, on a metal rail, or on conductive foam. Label any package that contains static-sensitive assemblies or components.
3. Discharge the static voltage from your body by wearing a wrist strap while handling these components. Servicing static-sensitive assemblies or components should be performed only at a static-free work station by qualified service personnel.
4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.
5. Keep the component leads shorted together whenever possible.
6. Pick up components by the body, never by the leads.
7. Do not slide the components over any surface.
8. Avoid handling components in areas that have a floor or work surface covering capable of generating a static charge.
9. Use a soldering iron that is connected to earth ground.

Use only special antistatic suction-type or wick-type desoldering tools.

Table 7-1: Static Discharge Susceptibility Levels

Semiconductor Classes	Relative Susceptibility Levels[a]
MOS or CMOS microcircuits or discretes or linear microcircuits with MOS inputs (Most Sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High frequency bipolar transistors	5
JFET	6
Linear microcircuits	7
Low power Schottky TTL	8
TTL (Least Sensitive)	9

[a] voltage equivalent for levels (voltage discharge from a 100 pF capacitor through resistance of 100Ω:

1 = 100 to 500 V	6 = 600 to 800 V
2= 200 to 500 V	7 = 400 to 1000 V (est)
3 = 250 V	8 = 900 V
4 = 500 V	9 = 1200 V
5 = 400 to 600 V	

Internal Fuse Replacement

Remove the SG 5050 from the power module.

WARNING

To avoid shock hazard, do not attempt to replace internal fuses with power applied to the SG 5050. Disconnect plug-in extender cables, if used, from the power module.

Remove the cabinet side panels, top rails and rear panel as described under Circuit Board Removal in this section.

WARNING

To avoid fire hazard, use only the fuse of correct type, voltage, and current rating as specified in Section 8 – Replacement Parts List.

The SG 5050 has eight internal fuses soldered on various circuit boards. After fuse replacement, reinstall the cabinet panels in reverse order of removal. The fuses are shown on the individual board schematics in Section 9.

CLEANING

This instrument should be cleaned as often as operating conditions require. Loose dust accumulated on the outside of the instrument can be removed with a soft cloth or a small brush. Remove dirt that remains with a soft cloth dampened in a mild detergent and water solution. Do not use abrasive cleaners.

Cleaning the interior of a unit should precede calibration since the cleaning processes could alter the settings of calibration adjustments. Use low velocity compressed air (approximately 5 lb/in^2) to blow off accumulated dust. Hardened dirt can be removed with a soft brush or cloth dampened in a solution of water and mild detergent.

CAUTION

To prevent damaging circuit boards and components, allow time for drying before applying power.

Avoid using chemical cleaning agents that might damage plastic parts. Avoid chemicals containing benzene, toluene, xylene, acetone or similar solvents.

REMOVAL INSTRUCTIONS

WARNING

To avoid shock or fire hazard, remove any extending cables from the power module before continuing.

Cabinet Side, Top and Rear Panel Removal

The side panels, top rails and rear panel will need to be removed for most repairs.

Side Cover Removal

The two side panels are snapped into the top and bottom rails of the SG 5050. To aid removal, there are cutouts at the rear corners of the covers. To remove, insert tweezers or a small straight-edged screwdriver into the cutout at the back edge of the cover, and carefully pry the cover away from the rail.

To replace covers, insert the front edge of the cover into the groove along the inside edge of the front frame assembly. Then press the cover down over the rails.

Release Latch Handle and Slider Removal

All plastic parts of the latch assemblies and the coil springs are individually replaceable. However, if latch tension spring becomes damaged, the attached bottom frame rail assembly must be replaced.

1. Remove the side covers from the SG 5050.

2. Pull the release latch handle out about 1/8" and hold.

3. Using a small screwdriver, move the release latch slider forward slightly while pushing down on the release latch handle with your finger to free the handle shaft from the slider. Pull out on the handle to remove.

4. To repair the release latch assembly, remove the bottom rail to which it is fastened. The rails are held with screws into the front and rear panel assemblies.

5. To replace the release latch handle, push the handle shaft through the slot in the front panel as far as it will go and hold it. Using a small screwdriver, move the release latch slider forward and the handle upward until the T-shaped end of the handle engages the end of the slider.

Rear Panel Removal

1. Remove side covers.

2. Remove the 4 screws holding the rear panel to the top frame assembly.

3. Remove the 4 guide studs holding the rear panel to the bottom chassis assembly. (Use a 3/16" hex wrench.)

4. Remove the rear panel.

5. Reassemble in reverse order.

Circuit Board Removal

The exploded-view drawing associated with the Replaceable Mechanical Parts list (at the rear of this manual) may be helpful in the removal or disassembly of individual components or subassemblies.

Plug-in Circuit Board Removal

The following boards are plugged into the A2 Interconnect Board (left to right, viewed from the rear):

Output Board (A4-A5)
DDS/VCO Boards (A2-A3)
CPU Board (A1)

To remove the plug-in boards:

1. Remove side covers.

2. Remove top rails and rear panel (as one unit) as follows:

   a. Remove the 6 screws that secure the top rails to the front casting.
   b. Remove the 3 screws from the center rail.
   c. Remove the 4 guide studs holding the rear panel to the bottom chassis assembly.

3. Unplug all cable connectors on the board, keeping track of cable orientation and socket location. Also refer to the SG 5050 basic block/cabling diagram in Section 9.

4. Carefully unplug and remove the desired board from the Interconnect Board.

NOTE

For troubleshooting purposes, boards can be reconnected with an Extender Board. Refer to Test Fixtures at the end of the Replaceable Mechanical Parts list for ordering information.

Troubleshooting of the circuit boards in the SG 5050 on an Extender Board (067-0175-00) is handled most easily with the use of flexible power module extender cables (067-0645-02). Three power module extender cables are required, and

in addition, the SG 5050 could be operated using GPIB commands with a GPIB extender cable (067-0996-00) attached to the SG 5050 CPU circuit board.

CAUTION

The SG 5050 should not be operated for an extended period of time outside the power module unless an external fan can supply sufficient air flow over the RF and Output circuit boards to keep the circuit board components from overheating.

WARNING

Heatsinks and power resistors on several of the SG 5050 circuit boards can become hot enough to cause skin burns.

A1 Front Panel Board Removal

1. Remove side covers.
2. Remove release latch handles.
3. Remove 12 screws holding front panel assembly to top and bottom frame assemblies.
4. Unplug the ribbon cable from the front of the A3 CPU Board. Unplug the two Output Head connector cables from the circuit boards. Pull the front panel assembly away from the top and bottom frame assemblies and unplug the two timebase cables from the front panel connectors. Note the locations of the coaxial cables at the front panel connectors for reconnection.
5. Remove 4 screws from the front panel board and lift the circuit board away from the front panel casting.
6. Reassemble in reverse order of removal.

A2 Interconnect Board Removal

1. Remove all five circuit boards that plug into the Interconnect Board.
2. Remove the hardware that secures the power transistor to the bottom frame assembly.
3. Remove the 6 screws that secure the A2 Interconnect Board and lift away from the bottom frame assembly.
4. Reassemble in reverse order of removal.

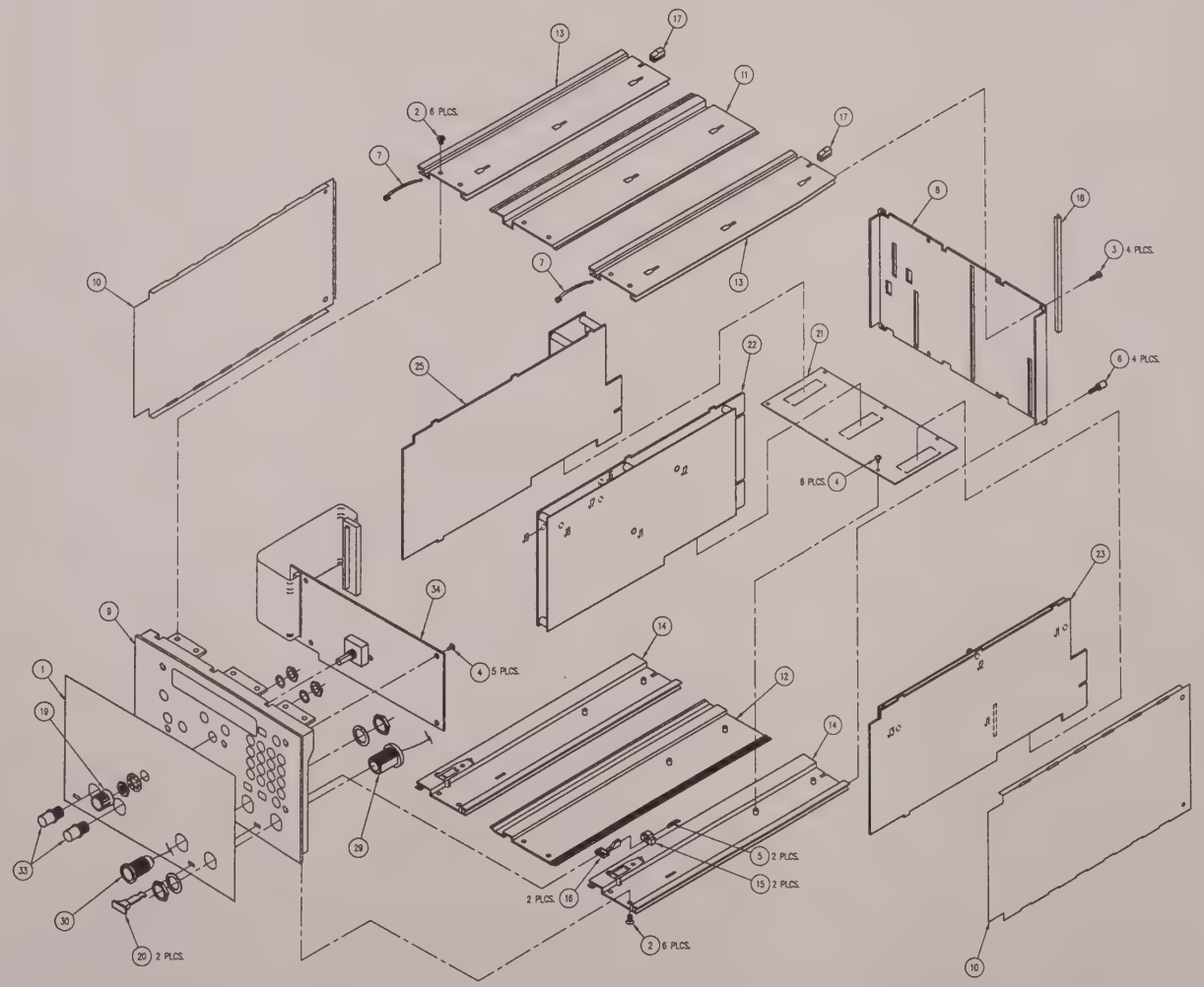
SECTION 8
REPLACEMENT PARTS LISTS

PARTS ORDERING INFORMATION

Replacement parts are ordered from TEGAM. The instrument part number, specific part number and description found on the assembly drawings are required.

PARTS LIST ENTRY DESCRIPTION

To locate a specific part, first locate the part on the schematic diagram, then look up the assembly drawing for that schematic (schematics are located in Section 9) in Section 8. Then, using the reference designator, e.g., U3, C1, etcetera, find the part number and description on the assembly drawing.



REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ECO #		

ITEM	QTY.	PART NO.	DESCRIPTION
35	1	96A08000	MANUAL, SG 5050 PROG. LEV. SINE WAVE GENERATOR
34	1	46B01600	PCB, FRONT PANEL
33	2	45B70000	CONN., BNC JACK
32	1	45B22300	TERMINAL HOUSING 10 CIRCUIT .100"
31	2	32C29700	S.A. CABLE, EXTERNAL TIMEBASE
30	1	32B27900	S.A. HARNESS, LEVELING HEAD
29	1	32C27800	S.A. CABLE, RF OUTPUT
28	1	32C27700	S.A. CABLE, HIGH FREQUENCY
27	1	32C27600	S.A. CABLE, LOW FREQUENCY
26	1	32C27500	S.A. CABLE, 10MHZ REFERENCE
25	1	31C34800	S.A. SG 5050 CPU BOARD W/ GPIB BOARD
24	1	31D29300	S.A. SG 5050 LEVELING HEAD
23	1	31D28600	S.A. SG 5050 OUTPUT DECK W/ OUTPUT AMP BOARD
22	1	31C24700	S.A. SG 5050 DDS BOARD W/ VCO BOARD
21	1	30C24001	S.A. PCB, SG 5050 CONNECTION BOARD
20	2	28B07200	KNOB, LATCH, IVORY
19	1	28B06700	KNOB, DOVE GRAY
18	18.7"	28B06400	PLASTIC CHANNEL .156" X .156"
17	2	28B06300	LOCKOUT, PLUG IN, PLASTIC
16	2	28B06200	BAR, LATCH RISE
15	2	28B04300	LATCH, RETAINING, SAFETY
14	2	23B08400	FRAME, SECT, CAB, BOTTOM
13	2	23B08300	FRAME, SECT, CAB, TOP
12	1	23B08200	SHIELD, ELEC., BOTTOM
11	1	23B08100	SHIELD, ELEC., TOP
10	2	23B08000	SHIELD, ELEC., SIDE
9	1	23B07800	SG 5050 FRONT PANEL REWORKED
8	1	23C07400	S.A. SG 5050 BACK PANEL, REWORKED
7	2	22B39400	CONTACT, ELEC. GROUNDING CUBE
6	4	22B39300	SUPPORT, PLUG IN
5	2	22B39200	SPRING, H.LEXT, .125"OD X .545", L, XLOOP
4	11	22B39100	SCREW, ASSEM WASHER
3	4	22B29400	SCREW, TPG., TR, #6-32 X .437"
2	12	20SM31FP	SCREW, #6-32 X 1/4", FLAT HEAD, PHILLIPS
1	1	19D26700	LABEL, SG 5050 FRONT PANEL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ±1/64 .XX± .010 .XXX± .005 ANGLES ±

DRAWN BY CA DATE 2-12-96
CHECKED BY DATE
APPROVED BY DATE
ISSUED DATE

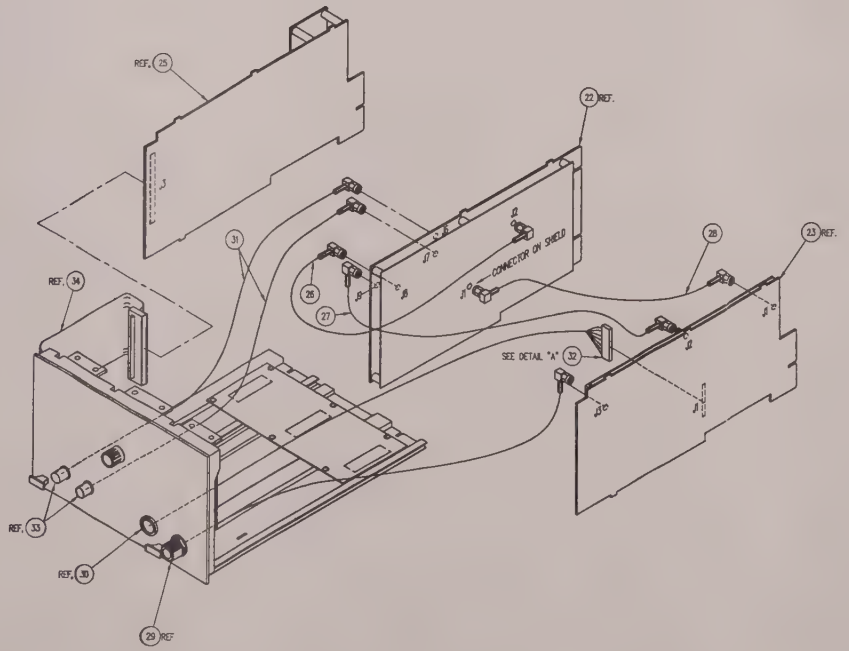
ASSY SG 5050 PROG. LEV. SINE WAVE GENERATOR

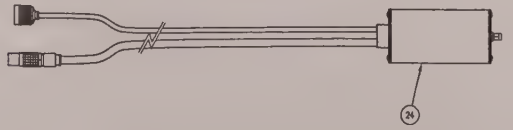
MATERIAL FINISH

SIZE D PROJECT NO. 96E014 PART NO. 33D30700 REV. A

DO NOT SCALE DRAWING SCALE 1=2 SHEET 1 OF 2

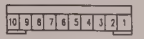
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	SEE SHEET 1 FOR REVISION LEVEL		





CONNECTOR PINOUT

PIN	WIRE COLOR
1	RED
2	BROWN/DRAIN
3	ORANGE
4	GRAY
5	GREEN
6	BLACK
7	PURPLE
8	YELLOW
9	WHITE
10	BLUE



DETAIL "A"

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ±1/64 .XX ± .010 ± .XXX ± .005

DRAWN BY CA DATE 2-12-98

DESIGNED BY DATE

APPROVED BY DATE

TECHNICAL DATE

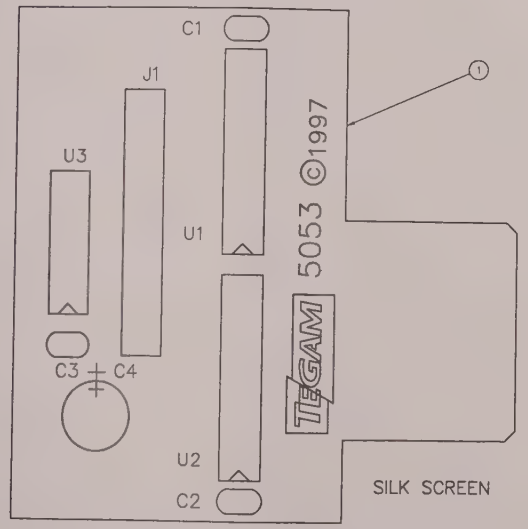
ASSY SG 5050 PROG. LEV. SINE WAVE GENERATOR

MATERIAL FINISH

COMMENTS COLOR

SIZE D PROJECT NO. 96CD14 PART NO. 33D30700 REV A

DO NOT SCALE DRAWING SCALE 1=2 SHEET 2 OF 2



SILK SCREEN

MicroDimensions, Inc.

TEGAM P/N 389505300
48C20601 2-18-97

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ECO #		

ITEM	QTY.	PART NO.	DESCRIPTION
C1-3	3	61B0890104	CAP 0.1UF 50V CERAMIC
C4	1	61B0650227	CAP 220UF 16V ,ALUM ELECT
U3	1	52900100	74LS00
U1	1	51B14100	IEEE 488 OCTAL GEN-PURPOSE TRANSCEIVER, 75160
U2	1	51B14000	IEEE 488 OCTAL GEN-PURPOSE TRANSCEIVER, 75161
1	1	48C20601	PCB, SG 5050 GPIB BOARD
J1	1	45B65200	INTERCONNECT STRIP, 26 POSITION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ±1/64 .XX ± .010 .XXX ± .005

DRAWN BY CA DATE 3-18-97
CHECKED BY DATE
APPROVED BY DATE
MATERIAL FINISH
WEIGHT RELEASE

S.A. PCB, SG 5050 GPIB BOARD

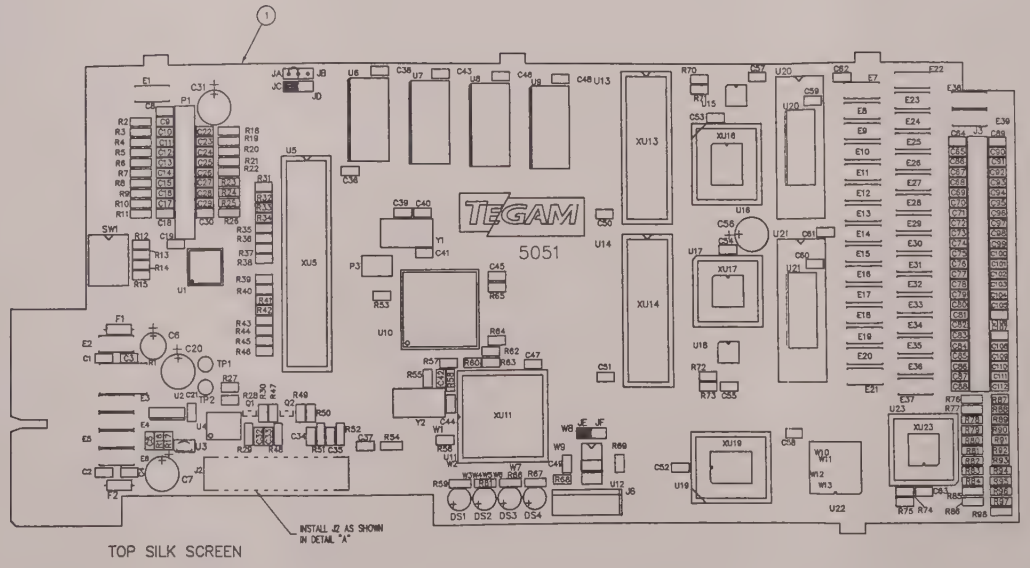
SIZE D | PROJECT NO. 96E014 | PART NO. 30D23200 | REV. A

DO NOT SCALE DRAWING

SCALE 4=1

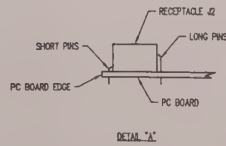
SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ECO #3511	2-27-97	CA
	B	ECO #3535	6-25-97	CA
	C	ECO #3538	7-10-97	CA
	D	ECO #3551	9-30-97	CA
	E	ECO #3591	1-13-98	CA
	F	ECO #		



TOP SILK SCREEN

TEGAM P/N 389505100 MicroDimensions, Inc. 48D20701 2-14-97



DETAIL "A"

ITEM	QTY	PART NO.	DESCRIPTION
U23	0	92837100	S.A. SG 5050 INTERRUPT CONTROLLER 22V10
U17	1	92837000	S.A. SG 5050 IO CONTROLLER 22V10
U11	1	92836901	S.A. 68306 16MHZ COMPANION CHIP, EPM7064
U5	1	92836800	S.A. FIRMWARE, SG 5050 LEVELED SINE WAVE EPROM
C6	1	61809000476	CAP 47UF 35V ,AL,TH ELECT.
C7,20, 31,56	4	61806650227	CAP 220UF 16V ,ALUM ELECT
U3	REF	56800600	REF 5V,LM336BZ5.0
DS1,2	2	55803100	LED,GREEN T 1 3/4 DIFFUSED
DS4	1	55803000	LED,YELLOW T 1 3/4 DIFFUSED
DS3	1	55802600	LED DISCRETE, T 1 3/4 RED HI EFFICIENCY
U13,14	2	53B08900	RAM W/BATTERY BACKUP MK48Z08-150 150NS
U12	REF	51B14400	MIC SUPERVISOR, MAX694
U20,21	REF	51B13800	8-DIGIT LED DISPLAY DECODER DRIVER, ICM7228A
P1	1	45865300	SOCKET STRIP, 26 POSITION
J2	1	45B65100	RECEPTACLE, AMPMODU, 2 ROW, 24 CIRCUIT, PCB RT.
JC,JE	2	45864100	JUMPER, 2 CIRCUIT, GOLD CONTACT, GRAY
J3	1	45843100	HEADER PCB .100"X.100" 2X25 50 CIRCUIT
TP1,2	2	45B18100	TEST POINT W/COLLAR ,BLACK
J6	1	45811400	HEADER .100"CENTER 7 CIRCUIT LOCKING RAMP
JC,JE	2	45810500	HEADER PCB .100"X.100" 1X3 3 CIRCUIT
P3	1	45808600	HEADER PCB .100"X.100" 2X3 6 CIRCUIT
XU5	1	45802600	SOCKET 40PIN DIP .6" PCB
XU13,14	2	45802500	SOCKET 28PIN DIP .6" PCB
W1-4	24"	44802205	WIRE #28 AWG SOLID KYNAR GREEN (4 PCS. - SEE SHT 2)
JA	.5"	44A01500	WIRE #22 AWG SOLID BUS, UNINSULATED, TINNED
SW1	1	42807600	SWITCH, PIANO-DIP 4 POSITION, SEALED
F1	1	41A07500	PICO FUSE 0.25A
F2	1	41A07400	PICO FUSE 3A
1	1	30023400	S.A. PCB, SG 5050 CPU BOARD SURFACE MOUNT COMP

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ±1/64 .XX± .010 ± .XXX± .005

DRAWN BY C.A. 2-10-97
ENGINEER APPROVED A.H. 2-20-97
APPROVED BY G. 2-27-97
REVISED CA 2-16-98
SIZE D PROJECT NO. 96ED74

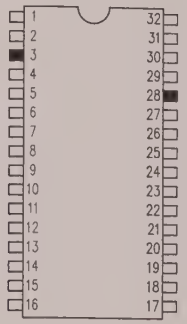
S.A. PCB, SG 5050 CPU BOARD

PART NO. 30023300 REV F

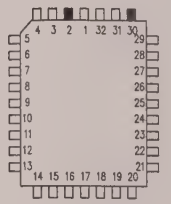
DO NOT SCALE DRAWING SCALE 2=1 SHEET 1 OF 2

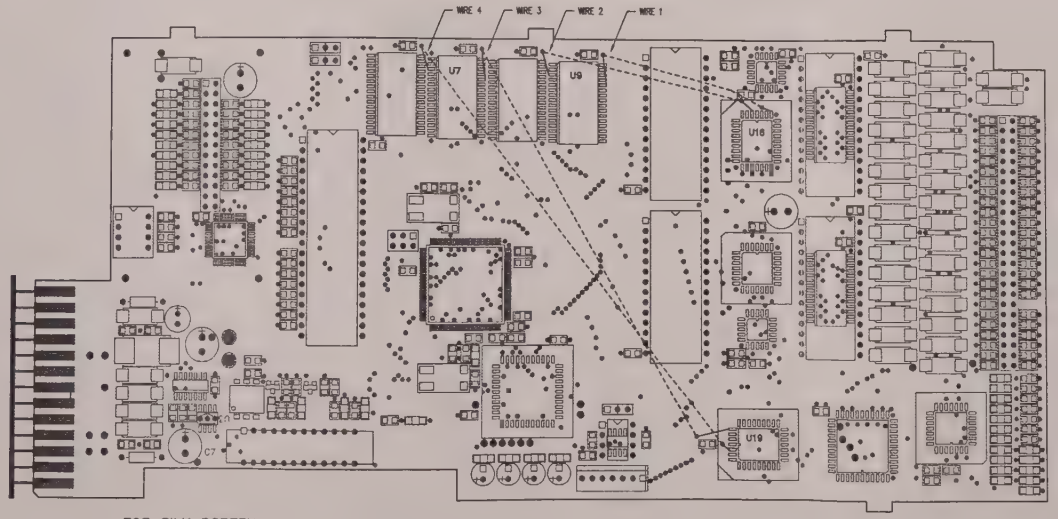
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	F	SEE SHEET 1 FOR REVISION LEVEL		

U7 & U9



U16 & U19





TOP SILK SCREEN

USING #28 AWG KYNAR WIRE (PART #44B02205)

1) CONNECT U16 PIN #30 TO U9 PIN #28
2) CONNECT U16 PIN #2 TO U9 PIN #3
3) CONNECT U19 PIN #30 TO U7 PIN #28
4) CONNECT U19 PIN #2 TO U7 PIN #3

NOTE:

ADDED WIRES SHOWN SOLID ARE ROUTED ON THE TOP (COMPONENT) SIDE OF BOARD.

ADDED WIRES SHOWN DASHED ARE ROUTED ON THE BACK (SOLDER) SIDE OF BOARD.

ADDED WIRES GO THROUGH THE BOARD THROUGH VIA HOLES BUT DO NOT CONNECT TO THE VIA. WIRE INSULATION PREVENTS CONNECTION.

TEGAM P/N 389505100 MicroDimensions, Inc. 48D20701 2-14-97

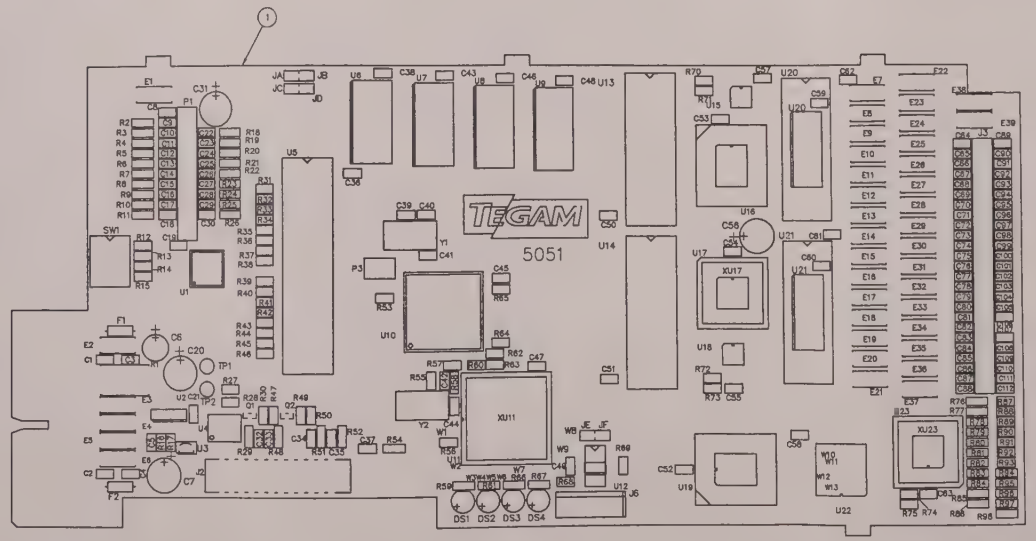
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ±1/64 .XX ± .010 .XXX ± .005 ANGLES ± 1°

DRAWN BY CA	DATE 2-10-97	S.A. PCB, SG 5050 CPU BOARD	
ENGINEER BY AJH	DATE 2-20-97		
APPROVED BY Q	DATE 2-27-97	MATERIAL	FINISH
RELEASED CA	DATE 2-16-97	ENGINEER	VALUE
SIZE D	PROJECT NO. 95ED14	PART NO. 30023300	REV. F
DO NOT SCALE DRAWING	SCALE 2=1	SHEET 2 OF 2	

ITEM	QTY.	PART NO.	DESCRIPTION
R28,31-46,56,60,63,70-73,87-93	31	60B3400103	RESISTOR 0805 CHIP, 10K OHM 1/16W 5%
R27	1	60B3400333	RESISTOR 0805 CHIP, 33K OHM 1/16W 5%
R1	1	60B3410478	RESISTOR WW 0.47 OHM 5% 2W
C39-42,44	5	61B1290100	CAP 0805 CHIP 10PF 50V 5% COG
C5,32-35,37,64-81,83-112	54	61B1290471	CAP 0805 CHIP 470PF 50V 5% COG
C1-4,8,19,21,36,38,43,45-55,57-63,82	29	61B1310104	CAP 0805 CHIP 0.1UF 50V 10% X7R
Y1	1	62B03900	CRYSTAL, 3.6864MHZ, 20PF
Y2	1	62B04000	CRYSTAL, 16.000MHZ, 20PF

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ECO #3911	2-25-97	Q
	B	ECO #3967	11-19-97	DDW
	C	ECO #		

R16	1	60B3400752	RESISTOR 0805 CHIP, 7.5K OHM 1/16W 5%
R12-15,30,47,49,50,53,55,57,62,64,65,68,69,74,75	18	60B3400472	RESISTOR 0805 CHIP, 4.7K OHM 1/16W 5%
R17	1	60B3400272	RESISTOR 0805 CHIP, 2.7K OHM 1/16W 5%
R58	1	60B3300104	RESISTOR 1206 CHIP, 100K OHM 1/8W 5%
R59,61,66,67	4	60B3380331	RESISTOR 1206 CHIP, 330 OHM 1/8W 5%
R2-11,18-28,29,48,51,52,54,76-86,94-98	40	60B3380181	RESISTOR 1206 CHIP, 180 OHM 1/8W 5%
U3	1	56B09900	REFERENCE 5.0V, LM336
U2	1	56B09800	VOLTAGE REGULATOR, UA723C
U4	1	55B04900	OPTO COUPLER, 4N35
U16,19	2	53B09200	EEPROM, 28C256, CMOS, 150NS PLCC-32
U8-9	REF	53B08400	RAM, 628512, 512K X 8, 70NS
U8-9	4	53B07700	RAM,628128,128K X 8,70NS LOW POWER
U12	1	51B14300	MIC SUPERVISOR, MAX694
U1	1	51B14200	IEEE 488 CONTROLLER DEVICE, 9OT7210
U18	REF	51B13900	4X DECODE COUNTER INTERFACE HCTL-2016
U15	1	51B13900	4X DECODE COUNTER INTERFACE HCTL-2016
U20,21	2	51B13700	8-DIGIT LED DISPLAY DECODER DRIVER, ICM7228A
U22	1	51B13600	PROGRAMMABLE PERIPHERAL INTERFACE, 82C55A
U10	1	51B13500	MICRO, MC68305, 16MHZ
Q1,2	2	50B06400	TRANSISTOR,MMBT4403,PNP
1	1	48D20701	PCB, SG 5050 CPU BOARD
XU11	1	45B64900	CHIP CARRIER SOCKET PLCC-44
XU13	0	45B63400	CHIP CARRIER SOCKET PLCC-28
XU17	1	45B63400	CHIP CARRIER SOCKET PLCC-28
E1-39	39	40B06700	FERRITE BEAD
ITEM	QTY.	PART NO.	DESCRIPTION



TOP SILK SCREEN

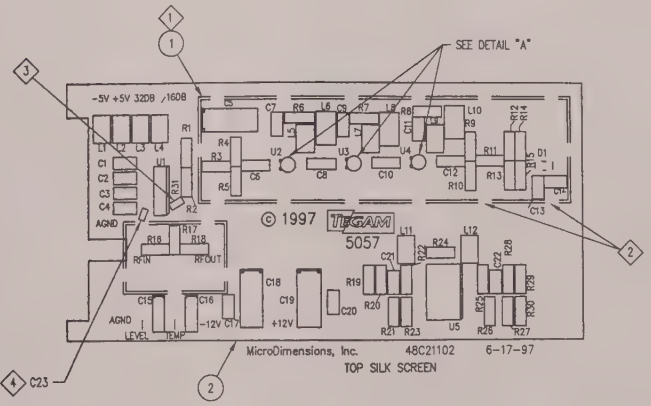
TEGAM P/N 389505100 MicroDimensions, Inc. 48D20701 2-14-97

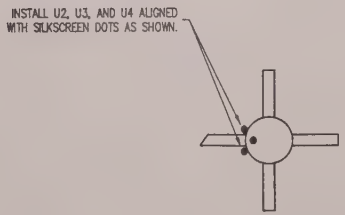
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ±1/64 XX±.010 ± .XXX±.005

DRAWN BY C.A.	DATE 2-18-97	S.A. PCB, SG 5050 CPU BOARD SURFACE MOUNT COMP
ENGINEER J.HURLBY	DATE 2-20-97	
APPROVED BY Q	DATE 2-25-97	MODEL
RELEASED C.A.	DATE 1-9-98	FINISH
SIZE D	PROJECT NO. 96E014	PART NO. 30023400 REV. C
DO NOT SCALE DRAWING	SCALE 2=1	SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	EO #3549	9-15-97	GI
	B	EO #3554	9-30-97	NLS
	C	EO #3559	11-18-97	NLS
	D	EO #3577	1-8-98	NLS
	E	EO #		

ITEM	QTY.	PART NO.	DESCRIPTION
C6,8, 10,12	4	61B1240104	CAP 1206 CHIP 0.1UF 50V 10% X7R
C23	1	61B1290101	CAP 0805 CHIP 100PF 50V 5% COG
C1-4, 7,9, 11,13, 14,17, 20-22	13	61B1310103	CAP 0805 CHIP 0.01UF 50V 10% X7R
C5,18, 19	3	61B1320106	CAP 7343H TANTALUM CHIP 10UF 35V 20%
C15,16	2	61B1350105	CAP 3216 TANTALUM CHIP 1UF 16V 20%





NOTES:

1. INSTALL SHIELD. WARNING: DO NOT SOLDER TO THE SHIELD COVER. REMOVE COVER AND CLEAN BOARD.
2. TRIM TWO TABS INDICATED ON REAR OF BOARD PRIOR TO SOLDERING. SOLDER THESE TWO TABS FROM FRONT OF BOARD ONLY.
3. SOLDER R31 BETWEEN PIN 1 OF U1 TO THE BOTTOM OF R2 LAYING IT FLAT.
4. SOLDER C23 BETWEEN PIN 14 OF U1 TO THE SHIELD GROUND PAD.

R31	1	60B3424999	RESISTOR 1206 CHIP, 49.9 OHM 1/8W 1%
R17	1	60B3423929	RESISTOR 1206 CHIP, 39.2 OHM 1/8W 1%
R16	1	60B3421409	RESISTOR 1206 CHIP, 14.0 OHM 1/8W 1%
R18	1	60B3421009	RESISTOR 1206 CHIP, 10.0 OHM 1/8W 1%
R3,11	2	60B3425768	RESISTOR 1206 CHIP, 5.76 OHM 1/8W 1%
R1,2, 4,5, 9,10, 12,13	8	60B3421741	RESISTOR 1206 CHIP, 1.74K OHM 1/8W 1%
R20,28	2	60B3380105	RESISTOR 1206 CHIP, 1M OHM 1/8W 5%
R23	1	60B3380204	RESISTOR 1206 CHIP, 200K OHM 1/8W 5%
R26,30	2	60B3380184	RESISTOR 1206 CHIP, 180K OHM 1/8W 5%
R19,24, 29	3	60B3380103	RESISTOR 1206 CHIP, 10K OHM 1/8W 5%
R21,27	2	60B3380102	RESISTOR 1206 CHIP, 1K OHM 1/8W 5%
R22	1	60B3380471	RESISTOR 1206 CHIP, 470 OHM 1/8W 5%
R25	1	60B3380680	RESISTOR 1206 CHIP, 68 OHM 1/8W 5%
R6-8	3	60B3380240	RESISTOR 1206 CHIP, 24 OHM 1/8W 5%
R14,15	0	60N0000000	NOT ASSIGNED
U1	1	54B12800	2-BIT ATTENUATOR, 16-32DB, AK002D2
U2-4	3	54B12400	BROADBAND RF AMPLIFIER, ERA-1
U5	1	54B11300	QUAD OP AMP, OP-470G
D1	1	50B07100	DIODE, DUAL RF DETECTOR, SMS3991-10
2	1	48C21102	PCB, SG 5050 LEVELING HEAD
L1-4, 11,12	6	40B06900	INDUCTOR, 1008 CHIP, 5.6UH 380MA
L6,8, 10	3	40B06800	INDUCTOR, 1812 CHIP, 6.8UH 285MA
L5,7, 9	3	31B26000	S.A. RF FILTER COIL
1	1	24B01100	SHIELD, CIRCUIT BOARD, 0.75" X 2.75" X 0.3"
ITEM	QTY.	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ±1/64 .XX± .010 ±0°30' .XXX± .005

DRAWN BY C.A.	DATE 7-9-97	S.A. PCB, SG 5050 LEVELING HEAD
CHECKED BY DOW	DATE 9-15-97	
APPROVED BY GI	DATE 9-15-97	MATERIAL / FINISH
REVISION C.A.	DATE 3-4-98	SHRINKAGE / COLOR
SIZE C	PROJECT NO. 96E014	PART NO. 30C23501 REV. E
DO NOT SCALE DRAWING	SCALE 2=1	SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	C	SEE SHEET 2 FOR REVISION LEVEL		

ITEM	QTY.	PART NO.	DESCRIPTION
C54	1	61B1310472	CAP 0805 CHIP 4700PF 50V 10% X7R
C32-35, 52	5	61B1310103	CAP 0805 CHIP 0.01UF 50V 10% X7R
C1-4, 6,7, 9,12-15,18, 19,21, 25,28, 29,37, 38,41, 43,44, 48-51, 56,57, 61,63, 66,72, 78-81, 86,88, 89,95, 97-108, 110,112, 113,116, 117,120, 121	59	61B1310104	CAP 0805 CHIP 0.1UF 50V 10% X7R
C5,8, 10,11, 16,17, 24,26, 27,30, 36,53, 58-60, 62,64, 65,67-71,73, 74,82, 87	27	61B1330106	CAP 7343H TANTALUM CHIP 10UF 35V 20%
C123	1	61B1370108	CAP, MICROWAVE, 0805, 1.0PF +/-0.1PF, 100V

ITEM	QTY.	PART NO.	DESCRIPTION
R4,7	2	60B3380222	RESISTOR 1206 CHIP, 2.2K OHM 1/8W 5%
R36,38	2	60B3380622	RESISTOR 1206 CHIP, 6.2K OHM 1/8W 5%
R63,64	2	60B3380752	RESISTOR 1206 CHIP, 7.5K OHM 1/8W 5%
R2,5, 10,17, 18,27, 31,33, 34,37, 39,40, 48,49	14	60B3380103	RESISTOR 1206 CHIP, 10K OHM 1/8W 5%
R42	1	60B3380333	RESISTOR 1206 CHIP, 33K OHM 1/8W 5%
R55,56, 59,60	4	60B3380623	RESISTOR 1206 CHIP, 62K OHM 1/8W 5%
R84	1	60B3381240	RESISTOR 0805 CHIP, 124 OHM 1/16W 1%
R82	1	60B3392490	RESISTOR 0805 CHIP, 249 OHM 1/16W 1%
R83	1	60B3425490	RESISTOR 1206 CHIP, 549 OHM 1/8W 1%
R79	1	60B3425620	RESISTOR 1206 CHIP, 562 OHM 1/8W 1%
R80,81	2	60B3421741	RESISTOR 1206 CHIP, 1.74K OHM 1/8W 1%
R68,70	2	60B3421002	RESISTOR 1206 CHIP, 10.0K OHM 1/8W 1%
R65,66	2	60B3423322	RESISTOR 1206 CHIP, 33.2K OHM 1/8W 1%
R22,23, 25	3	60B3421659	RESISTOR 1206 CHIP, 16.5 OHM 1/8W 1%
C42,46, 48,83-85,90-94	0	61N0000000	NOT ASSIGNED
C23,31	2	61B1290100	CAP 0805 CHIP 10PF 50V 5% COG
C55	1	61B1290271	CAP 0805 CHIP 270PF 50V 5% COG
C20,22, 39,40	4	61B1290102	CAP 0805 CHIP 1000PF 50V 5% COG
C109,111, 114,115, 118,119, 122	7	61B1310102	CAP 0805 CHIP 0.001UF 50V 10% X7R

R1,11, 14,20, 24	5	60B3380102	RESISTOR 1206 CHIP, 1K OHM 1/8W 5%
R41,43, 44,47, 50,53, 54,57	8	60B3380511	RESISTOR 1206 CHIP, 510 OHM 1/8W 5%
R71,72	2	60B3380331	RESISTOR 1206 CHIP, 330 OHM 1/8W 5%
R30,45, 46,51, 52,69, 73-78, 85-93	21	60B3380101	RESISTOR 1206 CHIP, 100 OHM 1/8W 5%
R29,58, 62,67	0	60N0000000	NOT ASSIGNED
AT3	1	54B12700	FIXED ATTENUATOR, 5DB
AT1	1	54B12600	FIXED ATTENUATOR, 2DB
AT2	1	54B12500	FIXED ATTENUATOR, 10DB
U13	1	54B12300	PLL FREQUENCY SYNTHESIZER, Q3236
U16-18	3	54B07100	OP AMP OP-27G
U15	1	54N00000	NOT ASSIGNED
U14	1	52B28000	MC10115, MECL QUAD LINE RECEIVER
U10	1	52B27600	74HC138, SHIFT REGISTER
U1,2	2	52B27200	7407, HEX BUFFER, OPEN COLLECTOR
U5,7	2	51B14900	GAAS FET SWITCH DRIVER, SMD-119
D3	1	50B07000	DIODE, SCHOTTKY, MBRS140T3, 40V,1A
D4-7	4	50B06700	DIODE, POWER, SIG 1A, SMB
D1,2	2	50B06500	DIODE, DUAL SERIES BAV99 SIGNAL
Q10	1	50B06400	TRANSISTOR,MMBT4403,PNP
Q8,9	2	50B06300	TRANSISTOR,MMBT4401,NPN
1	1	48D20903	PCB, SG 5050 VCO BOARD
C47	1	45B69400	JUMPER, 0 OHM, 0805 CHIP
R67	1	45B68300	JUMPER, 0 OHM, 1206 CHIP
K1-4, 6-8	7	43B05500	RELAY, SPST, RF, SOLID STATE GAAS,SW-259
E1-19	19	40B06700	FERRITE BEAD

ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ±1/64 .XX ± .02 ± .XXX ± .005

DRAWN BY	C.A.	DATE	12-9-97
ENGINEERING BY	D.S.C.	DATE	1-15-98
APPROVED BY	GI	DATE	1-15-98
RELEASED	CA	DATE	4-30-98

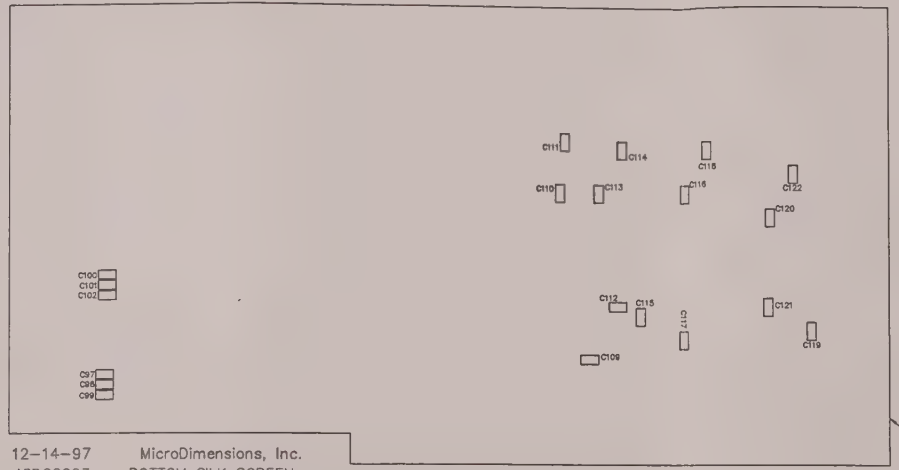
S.A. PCB, SG 5050 VCO BOARD SURFACE MOUNT COMP

MATERIAL | FINISH | ASSEMBLY | BLUE

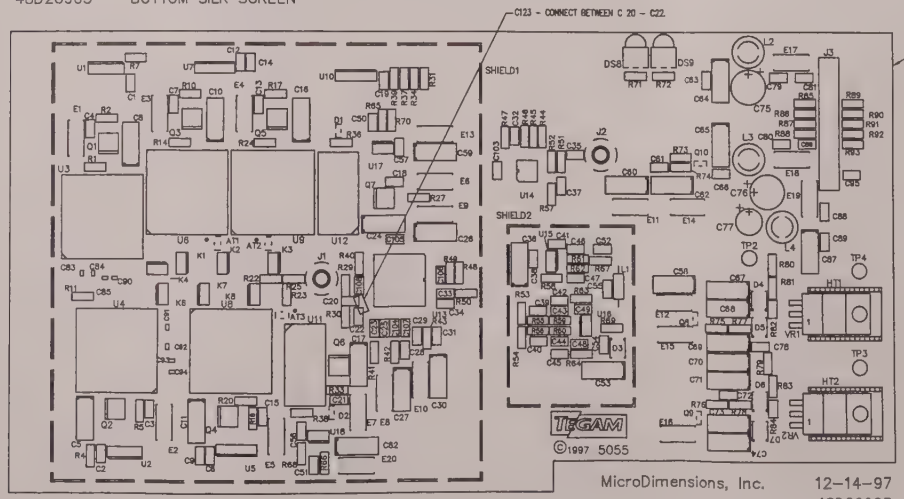
SIZE	PROJECT NO.	PART NO.	REV.
D	98ED14	30D23603	C

DO NOT SCALE DRAWING | SCALE 2=1 | SHEET 1 OF 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ECO 43087	1-15-98	CJ
	B	ECO 43815	3-31-98	MLS
	C	ECO		

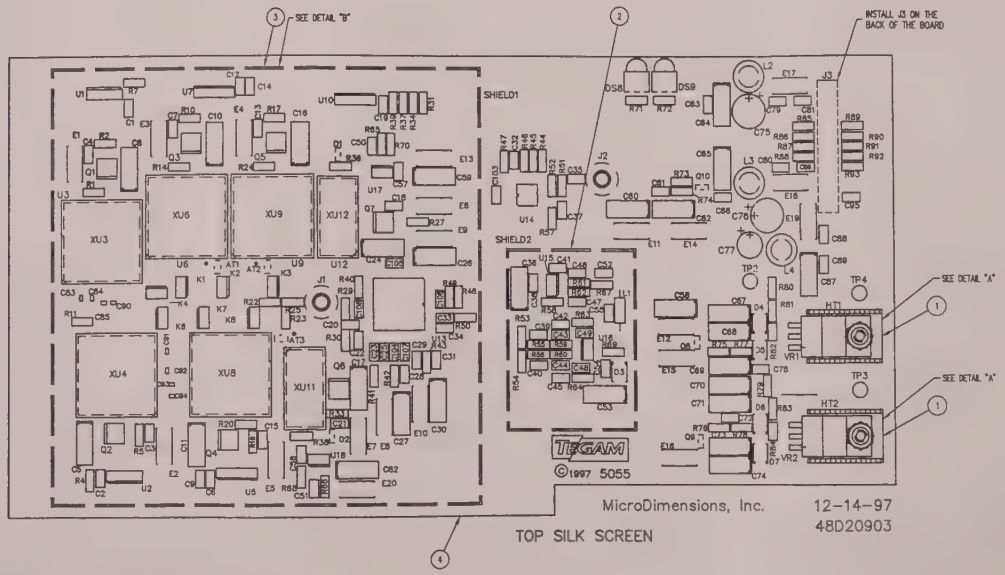


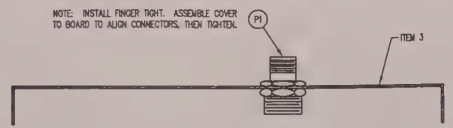
12-14-97 MicroDimensions, Inc.
48D20903 BOTTOM SILK SCREEN



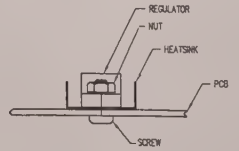
MicroDimensions, Inc. 12-14-97
48D20903
TOP SILK SCREEN

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ±1/64 .XX ± .010 .XXX ± .005			
	DRAWN BY C.A.	DATE 12-2-97	S.A. PCB, SG 5050 VCO BOARD SURFACE MOUNT COMP.
	CHECKED BY D.S.G.	DATE 1-15-98	
	APPROVED BY CJ	DATE 1-15-98	MATERIAL FINISH
	RELEASED CJ	DATE 4-27-98	DRAWING# VALUE
	SIZE D	PRODUCT NO. 95E014	PART NO. 30023803 REV. C
DO NOT SCALE DRAWING	SCALE 2=1		SHEET 2 OF 2





DETAIL "B"



DETAIL "A"

NOTES: ASSEMBLY SEQUENCE

1. SPACE CONNECTOR J1 .020 FROM BOARD PRIOR TO SOLDERING.
2. INSTALL ALL COMPONENTS EXCEPT U3, U4, U6, U8, U11, U12, XU3, XU4, XU6, XU8, XU11, XU12
3. INSTALL SHIELD1 AND SHIELD 2. WARNING: DO NOT SOLDER TO THE SHIELD COVERS. REMOVE THE COVERS.
4. CLEAN THE BOARD.
5. INSTALL U3, U4, U6, U8, U11, U12, XU3, XU4, XU6, XU8, XU11, XU12 USING ROSIN CORE SOLDER. DO NOT CLEAN.

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ECO #3587	1-15-98	CJ
	B	ECO #3606	2-3-98	MLS
	C	ECO #3615	3-31-98	MLS
	D	ECO #3635	4-30-98	MLS
	E	ECO #		

U3	1	62905000	VOLTAGE CONTROLLED OSCILLATOR 1350-2400MHZ
U4	1	62904900	VOLTAGE CONTROLLED OSCILLATOR 650-1300MHZ
U6	1	62904800	VOLTAGE CONTROLLED OSCILLATOR 400-800MHZ
U8	1	62904700	VOLTAGE CONTROLLED OSCILLATOR 200-400MHZ
U9	1	62904600	VOLTAGE CONTROLLED OSCILLATOR 100-200MHZ
U11	1	62904500	VOLTAGE CONTROLLED OSCILLATOR 50-100MHZ
U12	1	62904400	VOLTAGE CONTROLLED OSCILLATOR 25-50MHZ, POS-50
C77	1	61909004 76	CAP 47UF 35V ,ALUM ELECT.
C75,76	2	61906502 27	CAP 220UF 16V ,ALUM ELECT
VR1,2	2	56804800	VOLTAGE REG,ADJ,LM317AT
DS9	1	55800900	LED,GREEN
DS8	1	55800700	LED,RED
Q1-7	7	50806900	HEXFET, IRFD9120, 100V 1A
J1	1	45870200	BLIND MATE PLUG P.C.B
P1	1	45870100	CONN., SMA TO BLIND MATE JACK/BULKHEAD MOUNT
J2	1	45867900	CONNECTOR, SMA JACK, STRAIGHT PCB
TP2-4	3	45818100	TEST POINT W/COLLAR ,BLACK
J3	1	45809600	HEADER PCB .100"X.100" 2X13 26 CIRCUIT
L1	1	40804100	CHOKE, 100UH 125MA AXIAL
L2-4	3	40804000	CHOKE, 33UH 2.0A RADIAL
4	1	30023603	S.A. PCB, SG 5050 VCO BOARD SURFACE MOUNT COMP
XU11,12	2	28804000	INSULATOR FOR VCO PCB MOUNTING
XU3,4, 6,8, 9	5	28803600	INSULATOR FOR VCO PCB MOUNTING
3	1	24801500	SHIELD, REWORKED
2	1	24801400	SHIELD, CIRCUIT BOARD, 1.25" X 1.75" X 0.3"
HT1,2	2	22A33500	HEATSINK,TO-202
HT1,2	2	20SM22PP	SCREW, #4-40 X 3/8", PAN HEAD, PHILLIPS
HT1,2	2	20NE2000	NUT, KEPS, SS, #4-40
1	A/R	18A00100	THERMAL COMPOUND
ITEM	QTY	PART NO.	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ±1/64 .XX ± .010 .XXX ± .005

DRAWN BY C.A. 12-9-97
DESIGNED BY D.S.V. 1-15-98
APPROVED BY D 1-15-98
RELEASED C.A. 5-11-98

S.A. PCB, SG 5050 VCO BOARD

SIZE D PROJECT NO. 96ED14 PART NO. 30023703 REV. E

DO NOT SCALE DRAWING SCALE 2=1 SHEET 1 OF 1

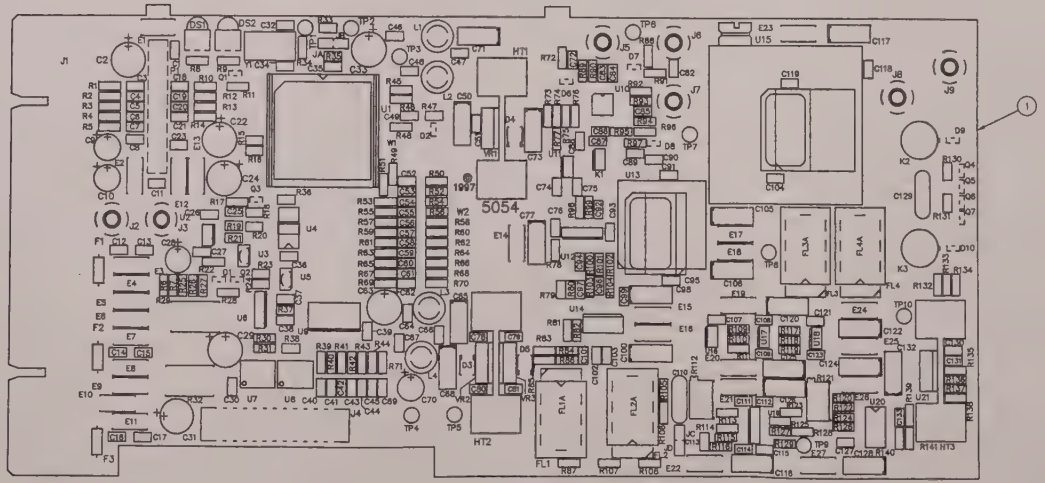
ITEM	QTY.	PART NO.	DESCRIPTION
C1,8, 11–17, 23,25, 27,35– 37,39, 46–48, 51,64, 66,67, 72,74– 76,78– 81,84, 86,91, 95,97, 99,101– 103,107– 109,111– 115,118, 121,123, 127,130, 131,133	55	8111313270X4	CAP 0805 CHIP 0.1UF 50V 10% X7R
C104,119	0	8111313270X4	CAP 0805 CHIP 0.1UF 50V 10% X7R
C50,65, 68,71, 73,77, 98,100, 105,106, 116,117, 120,122, 124–126, 128,132	19	81813207106	CAP 7343H TANTALUM CHIP 10UF 35V 20%
Y1	1	62B04300	CRYSTAL, 8.000MHZ, 20PF

ITEM	QTY.	PART NO.	DESCRIPTION
R37	1	60B3400752	RESISTOR 0805 CHIP, 7.5K OHM 1/16W 5%
R130,131	2	60B3400104	RESISTOR 0805 CHIP, 100K OHM 1/16W 5%
R79	1	60B3400684	RESISTOR 0805 CHIP, 680K OHM 1/16W 5%
R32	1	60B3410508	RESISTOR WW 0.47 OHM 5% 2W
R29	1	60B3410159	RESISTOR WW 1.5 OHM 5% 2W
R114	1	60B3421820	RESISTOR 1206 CHIP, 182 OHM 1/8W 1%
R115,128, 139	3	60B3424999	RESISTOR 1206 CHIP, 48.8 OHM 1/8W 1%
C32,34	2	6181290330	CAP 0805 CHIP 33PF 50V 5% COG
C3–7, 18–21, 40–45, 52–62, 69	27	6181290101	CAP 0805 CHIP 100PF 50V 5% COG
C26,30, 38	3	6181[illegible]0471	CAP 0805 CHIP 470PF 50V 5% COG
C49,82, 83,85, 87–90, 93,94, 96	11	6181310103	CAP 0805 CHIP 0.01UF 50V 10% X7R
C92	1	6181310472	CAP 0805 CHIP 4700PF 50V 10% X7R

ITEM	QTY.	PART NO.	DESCRIPTION
R74,75, 95,116, 117,120, 122,127, 135–138	12	60B3380102	RESISTOR 1206 CHIP, 1K OHM 1/8W 5%
R123,125	2	60B3380222	RESISTOR 1206 CHIP, 2.2K OHM 1/8W 5%
R109	1	60B3380302	RESISTOR 1206 CHIP, 3K OHM 1/8W 5%
R6,7, 11,22, 25–27, 31,45, 46,48, 50,52, 86,98, 110,111	17	60B3380103	RESISTOR 1206 CHIP, 10K OHM 1/8W 5%
R118,119	2	60B3380203	RESISTOR 1206 CHIP, 20K OHM 1/8W 5%
R99	1	60B3380223	RESISTOR 1206 CHIP, 22K OHM 1/8W 5%
R84	1	60B3380273	RESISTOR 1206 CHIP, 27K OHM 1/8W 5%
R30	1	60B3380333	RESISTOR 1206 CHIP, 33K OHM 1/8W 5%
R34,78	2	60B3380106	RESISTOR 1206 CHIP, 10M OHM 1/8W 5%
R133	1	60B3380829	RESISTOR 1206 CHIP, 8.2 OHM 1/8W 5%
R19	1	60B3392000	RESISTOR 0805 CHIP, 200 OHM 1/16W 1%
R80	1	60B3394021	RESISTOR 0805 CHIP, 4.02K OHM 1/16W 1%
R21	1	60B3394991	RESISTOR 0805 CHIP, 4.99K OHM 1/16W 1%
R15,16, 18,20, 23,24, 33,35, 36,38, 47	11	60B3400472	RESISTOR 0805 CHIP, 4.7K OHM 1/16W 5%

ITEM	QTY.	PART NO.	DESCRIPTION
R132,134	2	60B3380621	RESISTOR 1206 CHIP, 620 OHM 1/8W 5%
R72,76, 86–90, 92,93	7	60B3380511	RESISTOR 1206 CHIP, 510 OHM 1/8W 5%
R8,9	2	60B3380331	RESISTOR 1206 CHIP, 330 OHM 1/8W 5%
R87,108, 140	3	60B3380301	RESISTOR 1206 CHIP, 300 OHM 1/8W 5%
R124,126	2	60B3380221	RESISTOR 1206 CHIP, 220 OHM 1/8W 5%
R17,28	2	60B3380181	RESISTOR 1206 CHIP, 180 OHM 1/8W 5%
R1–5, 10,12– 14,39– 44,49, 51,53– 71,81– 83,85, 94,96, 97,103– 106	47	60B3380101	RESISTOR 1206 CHIP, 100 OHM 1/8W 5%
R91	1	60B3380430	RESISTOR 1206 CHIP, 43 OHM 1/8W 5%
R107	1	60B3380180	RESISTOR 1206 CHIP, 18 OHM 1/8W 5%
R100–102	3	60B3380150	RESISTOR 1206 CHIP, 15 OHM 1/8W 5%
R73,77, 113,141	0	60N0000000	NOT ASSIGNED
U3,5	2	56B09900	REFERENCE 5.0V, LM336
U6	1	56B09800	VOLTAGE REGULATOR, UA723C
U7,8	2	55B04900	OPTO COUPLER, 4N35
U12	1	54B12000	PLL FREQUENCY SYNTHESIZER, MC145170–1
U14	1	54B11900	DDS SYNTHESIZER, AD9850
U19	1	54B11700	WIDEBAND VARIABLE GAIN AMP CLC522
U2,17, 18	3	54B07100	OP AMP OP–27G
U10	1	52B28000	MC10115, MECL QUAD LINE RECEIVER
U9	1	52B27800	74HC244, SHIFT REGISTER
U11	1	51B14800	GAAS FET SWITCH DRIVER, SWD–109
U16	1	51B14700	D/A CONVERTER, LTC1451, 12–BIT
U4	1	51B14300	MIC SUPERVISOR, MAX694
D3–5	3	50B06700	DIODE, POWER, 1N4004 1A
D1,2, 6–10	7	50B06500	DIODE, DUAL SERIES BAV99 SIGNAL
Q2,3	2	50B06400	TRANSISTOR,MMBT4403,PNP
Q1,4–7	5	50B06300	TRANSISTOR,MMBT4401,NPN
1	1	48D20803	PCB, SC 5050 DDS BOARD
R129	1	45B68300	JUMPER, 0 OHM, 1206 CHIP
K1	1	43B04300	RELAY, SPDT,RF,SOLID STATE GAAS, SW–338
E1–27	27	40B06700	FERRITE BEAD
ITEM	QTY.	PART NO.	DESCRIPTION

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	A	EO #3549	9–15–97	Q
	B	EO #		



SILK SCREEN MicroDimensions, Inc. 48D20803 5–30–97

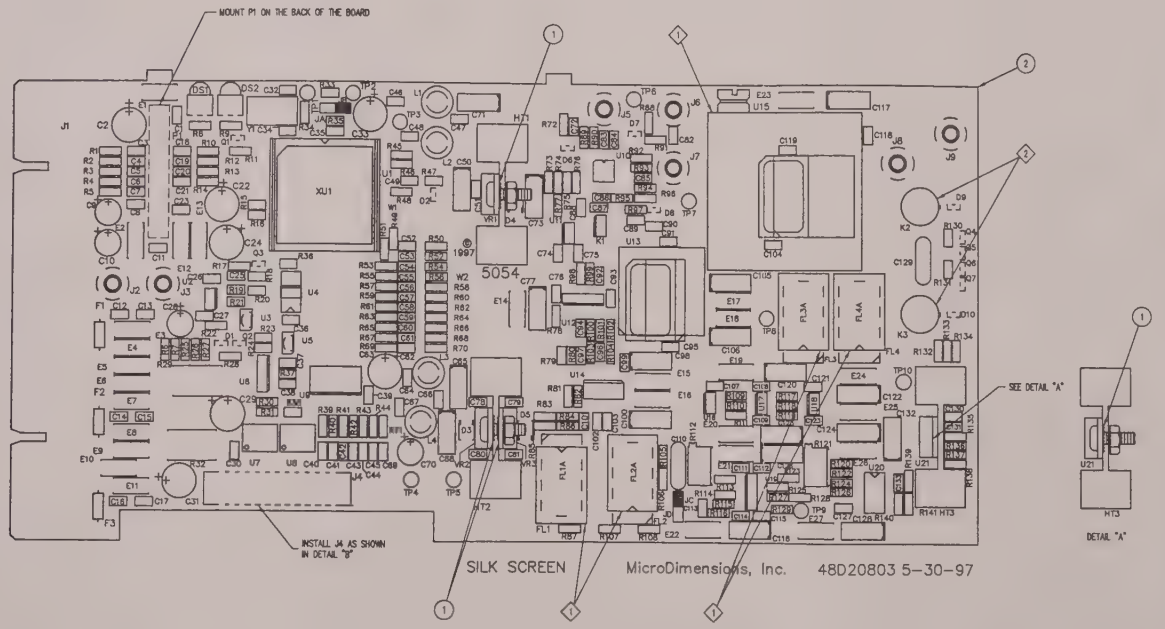
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS .XX±.01 .XXX±.005

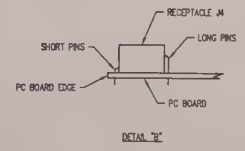
DRAWN BY	CA	6–12–97
ENGINEER	DVH	6–15–97
APPROVED BY	CJ	6–15–97
QA	CA	7–4–98

S.A. PCB, SC 5050 DDS BOARD
SURFACE MOUNT COMPONENTS

SIZE	PROJECT NO.	PART NO.	REV.
D	96E014	30023803	B

DO NOT SCALE DRAWING SCALE 2=1 SHEET 1 OF 1





DETAIL "B"

AMP OFFSET ADJUSTMENT:

A MEASURE OFFSET AT OUTPUT OF U21.

B SET FREQUENCY TO 0 AND AMPLITUDE TO 0. ADJUST R121 FOR 0 +/-5MV OFFSET.

C LEAVE FREQUENCY = 0 AND SET AMPLITUDE TO 4000. ADJUST R112 FOR 0 +/-5MV OFFSET.

NOTES: ASSEMBLY SEQUENCE

1. SPACE OFF OF THE BOARD 0.030.
   INSTALL ALL COMPONENTS EXCEPT K2 AND K3. CLEAN THE BOARD.
2. MOUNT RELAY FLUSH TO BOARD, SOLDER RELAY CASE TO BOARD USING ROSIN CORE SOLDER. DO NOT CLEAN.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ED #2548	9-15-97	Q
	B	ED #2560	1-13-98	Q
	C	ED #		

U1	1	92B37400	S.A. FIRMWARE, SG 5050 [illegible]
U13	1	82B05400	VCXO 107.374179MHZ
U15	1	62B04200	HIGH PERFORMANCE CLOCK OSC. 10.000MHZ
C110,129	2	61B13403335	CAP 3.3UF 50V CERAMIC
C9,10, 26,70	4	61B09004?6	CAP 47UF 35V ,ALUM ELECT.
C2,72, 24,29, 31,33, 63	7	61B06502?7	CAP 220UF 16V ,ALUM ELECT
R112,121	2	80B28101033	POT 20 TURN PCB RT ANGLE 10K OHM
VR2	1	56B10400	REGULATOR, +15V, 7815
VR1	1	56B10300	REGULATOR, -15V, 7915
U3,5	REF	56B00600	REF 5V,LM336Z5.0
VR3	1	56B00400	REGULATOR +12V,7812
DS1,2	2	55B00900	LED,GREEN
U20	1	54B12100	AMPLIFIER, CURRENT FEEDBACK 120MHZ, EL2030C
U21	1	54B11800	AMPLIFIER, VIDEO DISTRIBUTION, EL2099C
U4	REF	51B14400	MIC SUPERVISOR, MAX694
J2,J3	0	45N00000	NOT ASSIGNED
J5,J6, J7,J8, J9	5	45B67900	CONNECTOR, SMA JACK, STRAIGHT PCB
P1	1	45B65300	SOCKET STRIP, 26 POSITION
J4	1	45B65100	RECEPTACLE, AMPMODII, 2 ROW, 24 CIRCUIT, PCB RT
XU1	1	45B62000	CHIP CARRIER SOCKET 52 POSITION
TP1-10	10	45B18100	TEST POINT W/COLLAR ,BLACK
J8,JC	2	45B16100	JUMPER TWO CIRCUIT
JA,JC	2	45B10500	HEADER PCB .100"X.100" 1X3 3 CIRCUIT
K2,3	2	43B03700	RELAY, DPDT, RF, DC TO 3GHZ, TO-5, 5V
F3	1	41A07400	PICO FUSE 3A
FL3	1	41B05200	FILTER, LOW PASS, DC TO 15MHZ, PLP-15
FL1,2, 4	3	41B05100	FILTER, LOW PASS, DC TO 32MHZ, PLP-30
F1,2	2	41A05000	PICO FUSE 1A
L1-4	4	40B04000	CHOKE, 33UH 2.0A RADIAL
2	1	30D23803	S.A. PCB, SG 5050 DDS BOARD SURFACE MOUNT COMP
HT1-3	3	22B29600	HEATSINK, VERTICAL 1.5"
HT1-3	3	20SM22PP	SCREW, #4-40 X 3/8", PAN HEAD, PHILLIPS
HT1-3	3	20NE2000	NUT, KEPS, SS, #4-40
1	A/R	18A00100	THERMAL COMPOUND
ITEM	QTY	PART NO.	DESCRIPTION

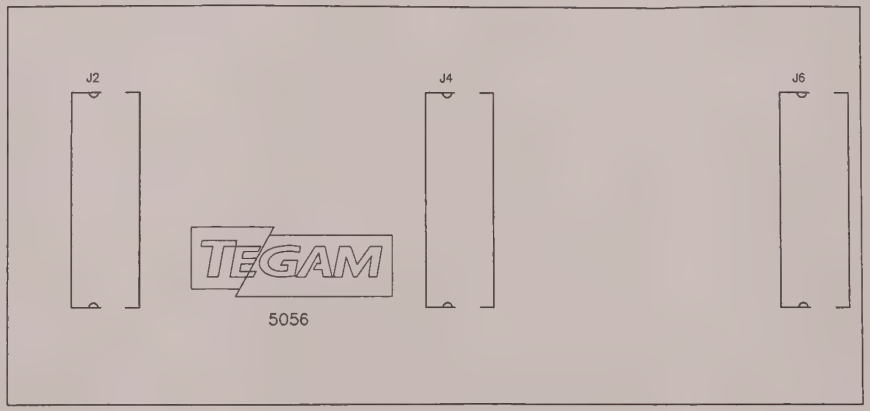
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS ±1/64 .XX ± .010 .XXX ± .005. ANGLES ±

DRAWN BY	DATE	S.A. PCB, SG 5050 DDS BOARD
CA	6-17-97	
CHECKED BY	DATE	
DDW	9-15-97	
APPROVED BY	DATE	MATERIAL / FINISH
Q	9-15-97	
RELEASED	DATE	COLOR
CA	2-4-98	

SIZE D | PRODUCT NO. 96E014 | PART NO. 30D23903 | REV. C

DO NOT SCALE DRAWING | SCALE 2=1 | SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	EO #		



SILK SCREEN MicroDimensions, Inc. 48C21001 4-14-97

ITEM	QTY.	PART NO.	DESCRIPTION
1	1	48C21001	PCB, SG 5050 CONNECTION BOARD
J2,J4, J6	3	45B65000	HEADER, AMPMODU, 2 ROW, 24 CIRCUIT, PCB

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ±1/64 .XX± .010 ±0°30' .XXX± .005

DRAWN BY C.A. DATE 7-8-97
CHECKED BY DATE
APPROVED BY DATE
REVISION DATE

S.A. PCB, SG 5050 CONNECTION BOARD

MATERIAL FINISH
SURFACE COLOR

SIZE C | PROJECT NO. 96E014 | PART NO. 30C24001 | REV. A

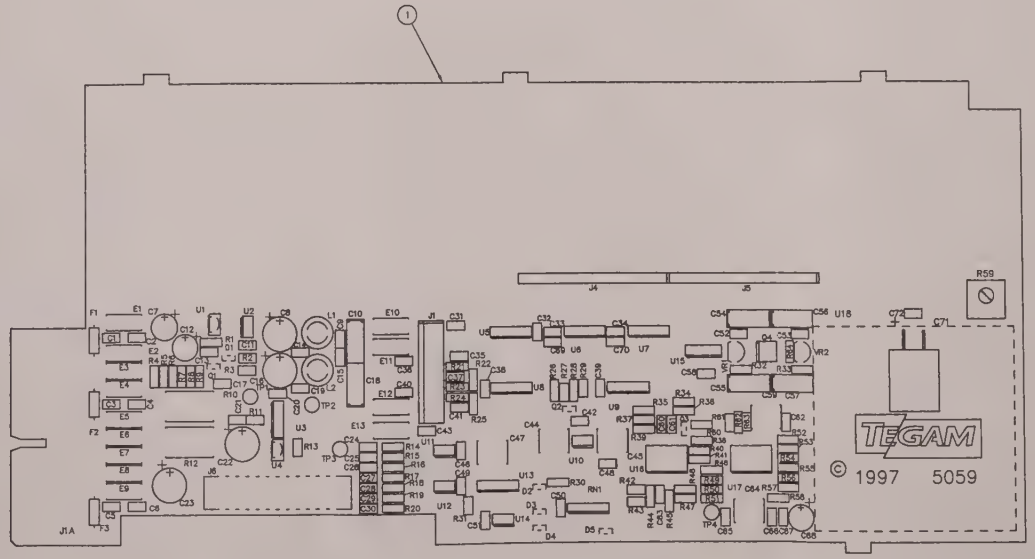
DO NOT SCALE DRAWING | SCALE 2=1 | SHEET 1 OF 1

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	A	ECO 03588	1-13-98	MLS
	B	ECO		

ITEM	QTY.	PART NO.	DESCRIPTION
C1–6, 9,13–15,17, 19,21, 31–34, 36,38–40,43, 50–53, 58,67, 69,70	30	61813101104	CAP 0805 CHIP 0.1UF 50V 10% X7R
C10,18, 54–57	6	61813201106	CAP 7343H TANTALUM CHIP 10UF 35V 20%
C44,45, 47,59, 64	5	61813601105	CAP 2225 CHIP 1.0UF 50V 10% X7R

ITEM	QTY.	PART NO.	DESCRIPTION
R52	1	60B3421501	RESISTOR 1206 CHIP, 1.50K OHM 1/8W 1%
R39	1	60B3428661	RESISTOR 1206 CHIP, 8.66K OHM 1/8W 1%
R1,4–6,37, 58,60, 47,50, 53,56, 64	14	60B3421002	RESISTOR 1206 CHIP, 10.0K OHM 1/8W 1%
RN1	1	60B3435002	RESISTOR NET SO-16 50K OHM X 8 ISO, 0.1%
C24–30, 37,41	9	61B1290101	CAP 0805 CHIP 100PF 50V 5% COG
C11,20	2	61B1290471	CAP 0805 CHIP 470PF 50V 5% COG
C35,42, 46,48, 49,60– 63,65, 66,72	12	61B1310103	CAP 0805 CHIP 0.01UF 50V 10% X7R

ITEM	QTY.	PART NO.	DESCRIPTION
R21,30, 34,36, 41,62	6	60B3421001	RESISTOR 1206 CHIP, 1.0K OHM 1/8W 1%
R10	1	60B3410159	RESISTOR WW 1.5 OHM 5% 2W
R12	1	60B3410478	RESISTOR WW 0.47 OHM 5% 2W
R31	1	60B3400105	RESISTOR 0805 CHIP, 1M OHM 1/16W 5%
R43	1	60B3400684	RESISTOR 0805 CHIP, 680K OHM 1/16W 5%
R29,42, 61,63	4	60B3400104	RESISTOR 0805 CHIP, 100K OHM 1/16W 5%
R27	1	60B3400333	RESISTOR 0805 CHIP, 33K OHM 1/16W 5%
R11	1	60B3400752	RESISTOR 0805 CHIP, 7.5K OHM 1/16W 5%
R13	1	60B3400772	RESISTOR 0805 CHIP, 2.7K OHM 1/16W 5%
R2	1	60B3394991	RESISTOR 0805 CHIP, 4.99K OHM 1/16W 1%
R3	1	60B3382000	RESISTOR 0805 CHIP, 200 OHM 1/16W 1%
R26	1	60B3380563	RESISTOR 1206 CHIP, 56K OHM 1/8W 5%
R28,44, 49,55	4	60B3380473	RESISTOR 1206 CHIP, 47K OHM 1/8W 5%
R46,48, 51,57	4	60B3380822	RESISTOR 1206 CHIP, 8.2K OHM 1/8W 5%
R35,45	2	60B3380472	RESISTOR 1206 CHIP, 4.7K OHM 1/8W 5%
R54	1	60B3380122	RESISTOR 1206 CHIP, 1.2K OHM 1/8W 5%
R60	1	60B3380112	RESISTOR 1206 CHIP, 1.1K OHM 1/8W 5%
R9	1	60B3380181	RESISTOR 1206 CHIP, 180 OHM 1/8W 5%
R14–19, 20,22–25	11	60B3380101	RESISTOR 1206 CHIP, 100 OHM 1/8W 5%
R32,33, 58	3	60B3380150	RESISTOR 1206 CHIP, 15 OHM 1/8W 5%
U14	1	56810800	REFERENCE 5.0V, LT1019
U1,4	2	56809900	REFERENCE 5.0V, LM336
U3	1	56909800	VOLTAGE REGULATOR, UA723C
U10	1	54812900	DUAL OP AMP, LM6172
U16,17	2	54811300	QUAD OP AMP, OP-470G
U5	1	54811200	DRIVER,SINKING 7 CHANNEL, ULN2003
U2	1	54807100	OP AMP OP-27G
U15	1	52928300	74HC00, SHIFT REGISTER
U8,9	2	52827700	74HC595, SHIFT REGISTER
U13	1	51815100	D/A CONVERTER, LTC1594, 12 BIT
U11,12	2	51815000	A/D CONVERTER, LTC1446, DUAL 12 BIT
U6,7	2	51814900	GAAS FET SWITCH DRIVER, SWD-119
Q2,3	2	50807200	MOSFET, 2N7002 N-CHANNEL ENHANCEMENT
D1–5	5	50806500	DIODE, DUAL SERIES BAV99 SIGNAL
Q1	1	50806400	TRANSISTOR,MMBT4403,PNP
1	1	48D21902	PCB, SG 5050 OUTPUT DECK BOARD
E1–13	13	40806700	FERRITE BEAD
ITEM	QTY	PART NO.	DESCRIPTION



TOP SILK SCREEN
MicroDimensions, Inc. 48D21902 12-8-97

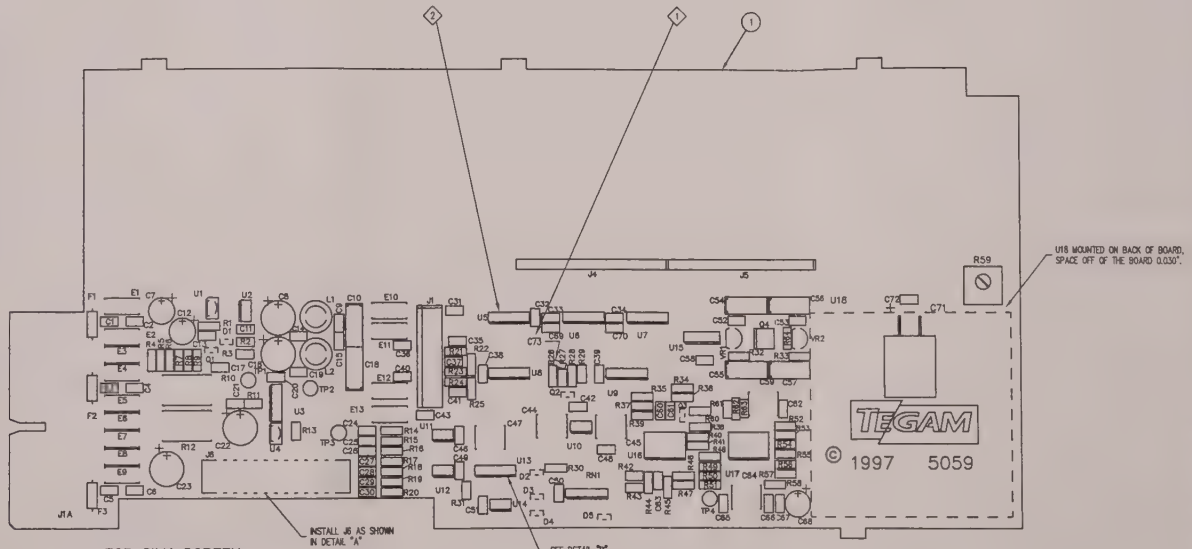
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ±1/64 .XX ± .010 .XXX ± .005 ANGLES ± 2°

DRAWN BY	C.A.	12-2-97
ENGINEER BY	D.S.C.	1-13-98
APPROVED BY	M.L.S.	1-13-98
RELEASED	C.A.	2-5-98

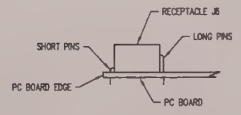
S.A. PCB, SG 5050 DECK BOARD SURFACE MOUNT COMP

SIZE D | PROJECT NO. 96ED14 | PART NO. 30D24702 | REV. B

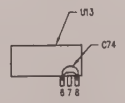
DO NOT SCALE DRAWING | SCALE 2=1 | SHEET 1 OF 1



TOP SILK SCREEN
MicroDimensions, Inc. 48D21902 12-8-97



DETAIL "A"



DETAIL "B"

NOTES:

1. C73 IS SOLDERED BETWEEN TOP OF R26 AND TOP OF R27 AS SHOWN.
2. CUT OFF U5 PIN #8.

REVISIONS				
ECN#	LTR	DESCRIPTION	DATE	APPROVED
	A	SD #3588	1-13-98	MLS
	B	SD #		

ITEM	QTY.	PART NO.	DESCRIPTION
C73	1	61B1310103	CAP, 0805 CHIP, 0.01UF, 10%, X7R
C71	1	61B1100337	CAP, 330UF, 35V, ALUM ELECT.
C7,12, 68	3	61B0900476	CAP, 47UF, 35V, ALUM ELECT.
C8,16, 22,23	4	61B0650227	CAP, 220UF, 16V, ALUM ELECT
C74	1	61B0030104	CAP, .1UF, 50V, CERAMIC
R59	1	60B2530203	POT,ST, CERMET, PCB, 20K OHM
VR1,2	2	56B10700	VOLTAGE REGULATOR, TL750L05
U18	1	56B10600	DC/DC CONVERTER, 9-36V TO +15V, 1A, ISOLATED
Q4	1	50B06900	HEXFET, IRFD9120, 100V, 1A
J6	1	45B65100	RECEPTACLE, AMPMODU, 2 ROW, 24 CIRCUIT, PCB RT.
J4,J5	2	45B47800	HEADER, .100" CENTER, 15 POSITION
J1	1	45B21900	HEADER, 10 CIRCUIT, .100" FRICTION LOCK
TP1-4	4	45B18100	TEST POINT W/COLLAR, BLACK
F3	1	41A07400	PICO FUSE, 3A
F1,2	2	41A05000	PICO FUSE, 1A
L1,2	2	40B04000	CHOKE, 33UH, 2.0A RADIAL
1	1	30D24702	S.A. PCB, SG 5050 DECK BOARD SURFACE MOUNT COMP

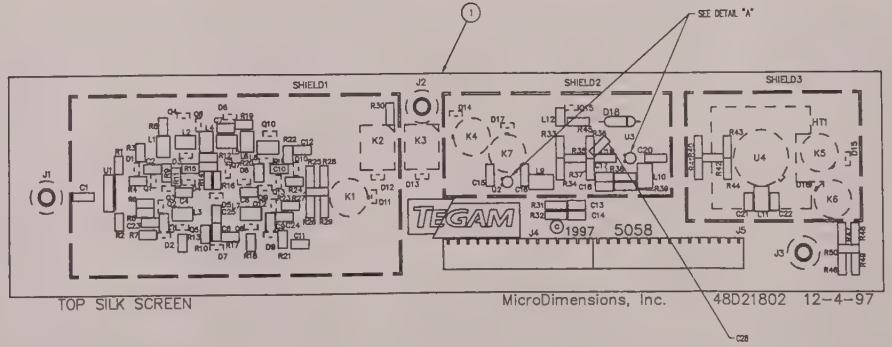
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ±1/64 .XX ±.010 .XXX ±.005 DECIMALS ±.005 ANGLES ±1°

DRAWN BY C.A.	DATE 12-8-97	S.A. PCB, SG 5050 DECK BOARD
CHECKED BY D.S.C.	DATE 1-13-98	
ENGINEERING M.S.	DATE 1-13-98	APPROVAL / DATE
MFG/QA C.A.	DATE 2-5-98	
SIZE D	PROJECT NO. 96ED14	PART NO. 30D24802 REV. B
DO NOT SCALE DRAWING	SCALE 2=1	SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ED #3592	1-13-98	MLS
	B	ED #3822	4-2-98	MLS
	C	ED #		

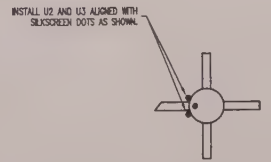
ITEM	QTY.	PART NO.	DESCRIPTION
R27,35, 42	3	60B3425768	RESISTOR 1206 CHIP, 5.76 OHM 1/8W 1%
C26	1	6181220188	CAP 1206 CHIP 1.0PF 100V 5% COG
C1,15, 16,19, 20	5	6181240104	CAP 1206 CHIP 0.1UF 50V 10% X7R
C13,17	2	6181290100	CAP 0805 CHIP 10PF 50V 5% COG
C3,6, 9	3	6181290680	CAP 0805 CHIP 68PF 50V 5% COG
C22	1	6181290101	CAP 0805 CHIP 100PF 50V 5% COG
C2,4, 5,7, 8,10- 12	8	6181290102	CAP 0805 CHIP 1000PF 50V 5% COG
C14,18, 21	3	6181310103	CAP 0805 CHIP 0.01UF 50V 10% X7R
C23,24	2	6181370188	CAP, MICROWAVE, 0805, 1.8PF +/-0.1PF, 100V
C25	1	6181370568	CAP, MICROWAVE, 0805, 5.6PF +/-0.1PF, 100V

R25,26, 28,29, 33,34, 36,37, 40,41, 43,44	12	60B3421741	RESISTOR 1206 CHIP, 1.74K OHM 1/8W 1%
R3,7, 12,14, 15,17, 19,21, 22	9	60B3400683	RESISTOR 0805 CHIP, 68K OHM 1/16W 5%
R1,2, 4-6, 8-11, 13,18, 20,23, 24	14	60B3400103	RESISTOR 0805 CHIP, 10K OHM 1/16W 5%
R16	1	60B3400472	RESISTOR 0805 CHIP, 4.7K OHM 1/16W 5%
R30	1	60B3380102	RESISTOR 1206 CHIP, 1K OHM 1/8W 5%
R46-49	4	60B3380181	RESISTOR 1206 CHIP, 180 OHM 1/8W 5%
R31,32, 45	3	60B3380101	RESISTOR 1206 CHIP, 100 OHM 1/8W 5%
R50	1	60B3380750	RESISTOR 1206 CHIP, 75 OHM 1/8W 5%
R38,39	2	60B3380680	RESISTOR 1206 CHIP, 68 OHM 1/8W 5%
U2,3	2	54B13200	BROADBAND RF AMPLIFIER, ERA-5
U1	1	54B13100	VOLTAGE VARIABLE ATTENUATOR, 400MLAT-339
D4,8	2	50B08200	VARACTOR DIODE, SMV1204-04
D5	1	50B08100	VARACTOR DIODE, SMV1204-05
D6	1	50B08000	VARACTOR DIODE, SMV1202-12
D1,10	2	50B07900	VARACTOR DIODE, SMV1202-08
D3	1	50B07800	VARACTOR DIODE, SMV1200-104
D7	1	50B07700	VARACTOR DIODE, SMV1200-07
D2,9	2	50B07600	VARACTOR DIODE, SMV1200-04
Q1-6, 8-13, 15	13	50B07400	GAAS MMIC FET, AF002C1
Q7	1	50B07300	JFET, MMBF4393 N-CHANNEL DEPLETION
D11-17	7	50B06500	DIODE, DUAL SERIES BAV99 SIGNAL
1	1	48D21802	PCB, SG 5050 OUTPUT AMP BOARD
L3,7	2	40B07500	INDUCTOR, 1008 CHIP, 22NH 1000MA
L4,8	2	40B07300	INDUCTOR, 1008 CHIP, 470NH 470MA
L2,6	2	40B07200	INDUCTOR, 1008 CHIP, 120NH 650MA
L1,5	2	40B07100	INDUCTOR, 1008 CHIP, 56NH 1000MA
ITEM	QTY.	PART NO.	DESCRIPTION



TOP SILK SCREEN

MicroDimensions, Inc. 48D21802 12-4-97



DETAIL "A"

NOTE:

1. INSTALL U2 AND U3 AS SHOWN IN DETAIL "A", DO NOT TRIM THE LEADS ON U2 AND U3.
2. INSTALL C28 FROM THE JUNCTION OF R35 AND C19 TO GND ON THE TOP SIDE OF THE BOARD.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ±1/64 .XX ± .010 .XXX ± .005

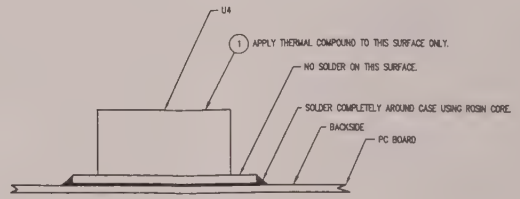
DRAWN BY C.A. 12-4-97
CHECKED BY M.S. 1-13-98
APPROVED BY M.L.S. 1-13-98
CA 6-1-98

S.A. PCB, SG 5050 AMP BOARD SURFACE MOUNT COMP.

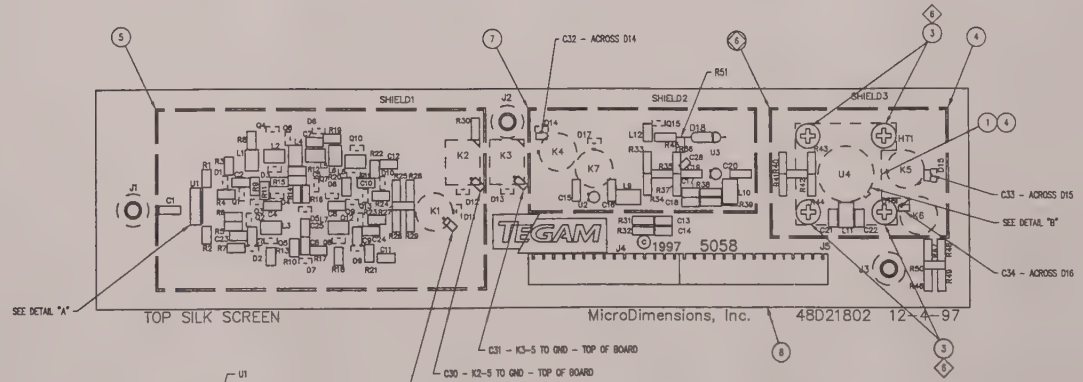
SIZE D PROJECT NO. 98C014 PART NO. 30D24902 REV. C

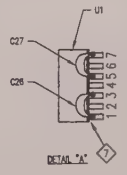
DO NOT SCALE DRAWING SCALE 2=1 SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ECN 97402	1-13-98	MLS
	B	ECN #		


U4
1 APPLY THERMAL COMPOUND TO THIS SURFACE ONLY.
NO SOLDER ON THIS SURFACE.
SOLDER COMPLETELY AROUND CASE USING ROSIN CORE.
BACKSIDE
PC BOARD

DETAIL "B"





NOTES: ASSEMBLY SEQUENCE

1. INSTALL SHIELD 1, 2, AND 3, COILS, CONNECTORS AND JACKS. WARNING. DO NOT SOLDER TO THE SHIELD COVERS. REMOVE COVERS AND CLEAN BOARD.
2. K1, K2, K3, K4, K5, K6, K7, U4 AND HT1 ARE INSTALLED ON THE BACK OF THE BOARD. THE CASES OF K1, K2, K3, K4, K5, K6, AND K7 ARE TO BE SOLDERED CONTINUOUSLY TO THE GROUND PLANE ON THE BACK OF THE BOARD USING ROSIN CORE SOLDER. K2 MUST BE INSTALLED BEFORE K3. DO NOT CLEAN. AFTER SOLDERING, CLIP LEADS AS FLUSH AS POSSIBLE TO THE SOLDER JOINT.
3. THE CASE OF U4 MUST BE SOLDERED CONTINUOUSLY TO THE GROUND PLANE ON THE BACK OF THE BOARD AS SHOWN IN DETAIL "B" USING ROSIN CORE SOLDER. INSURE PART IS FLUSH TO THE BOARD. DO NOT CLEAN.
4. INSTALL HT1 OVER U4 USING THERMAL COMPOUND.
5. SOLDER R51 FROM JUNCTION OF R45/D18 TO TOP OF R36.
6. APPLY LOCKTITE RC609 TO SCREWS.
7. CAP LEADS MUST BE AS SHORT AS POSSIBLE.

ITEM	QTY	PART NO.	DESCRIPTION
C29-33	8	61812901O1	CAP 0805 CHIP 100PF 50V 5% COG
C26,27	2	6180330153	CAP .015UF 50V CERAMIC
R51	1	6083380821	RESISTOR 1206 CHIP, 820 OHM 1/8W 5%
D18	1	56804000	SCHOTTKY DIODE,1N5711
U4	1	54813300	RF POWER AMPLIFIER, AR2569, TO-8
K2,3	2	54813000	ATTENUATOR RELAY, 2008, A150-20-5
J4,J5	2	45868400	RECEPTACLE, 15 CIRCUIT .100" PCB BOTTOM ENTRY
J1,J2, J3	3	45867900	CONNECTOR, SMA JACK, STRAIGHT PCB
L12	.1"	44802100	WIRE #28 AWG SOLID BUS
K1,4-7	5	43803700	RELAY, DPDT, RF, DC TO 3GHZ, TO-5, 5V
L8-11	3	31826000	S.A. RF FILTER COIL
8	1	30D24902	S.A. PCB, SG 5050 AMP BOARD SURFACE MOUNT COMP
7	1	24801000	SHIELD, CIRCUIT BOARD, 1.00" X 2.25" X 0.3"
6	1	24800900	SHIELD, CIRCUIT BOARD, 1.25" X 1.75" X 0.3"
5	1	24800500	SHIELD, CIRCUIT BOARD, 1.75" X 3.25" X 0.3"
4	1	23806300	HEATSINK, FABRICATED BLOCK, R.F. AMPLIFIER
3	6	20SM229P	SCREW, #4-40 X 3/8", PAN HEAD, PHILLIPS
1	A/R	18A02100	THERMAL COMPOUND

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCED ARE: FRACTIONS ±1/64 .X ±.010 .XX ±.005 .XXX ±.005 ANGLES ±1°

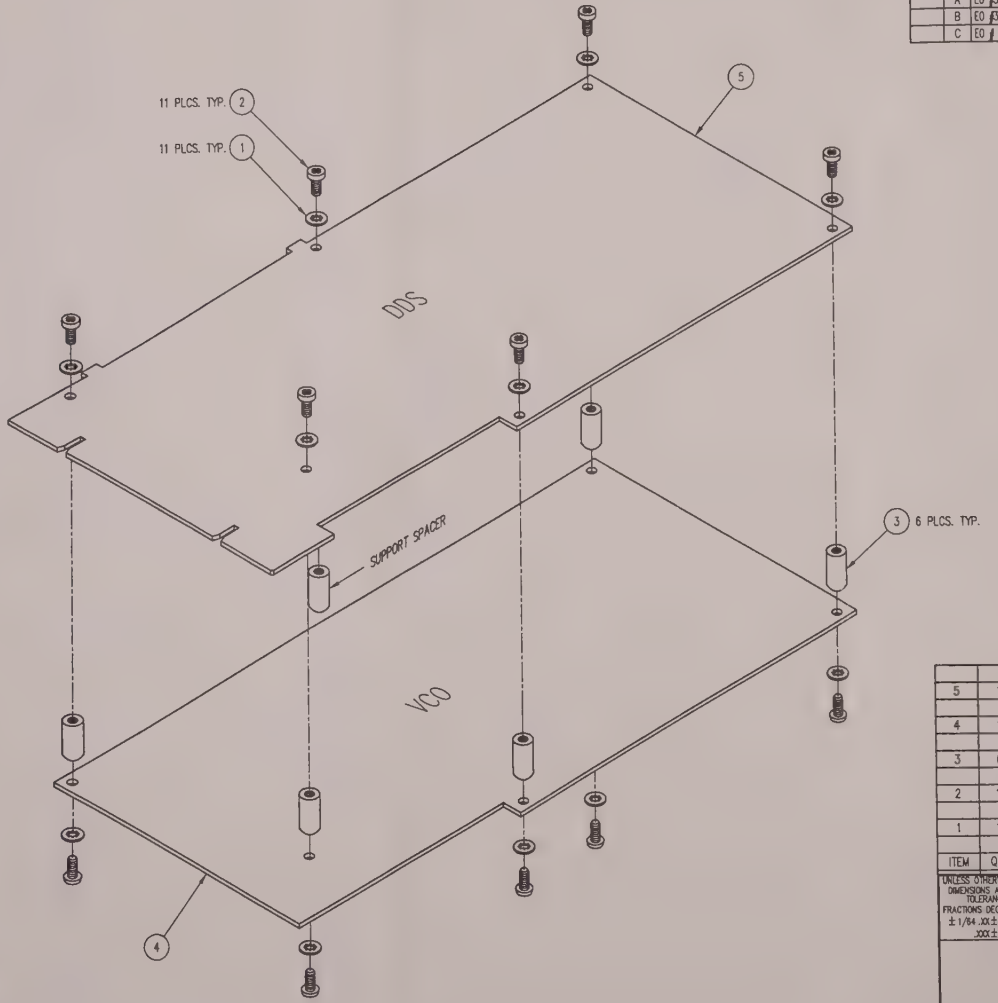
	NAME	DATE
DRAWN BY	C.A.	12-3-97
DESIGNED BY	M.S.	1-13-98
APPROVED BY	M.S.	1-13-98
RELEASED	C.A.	2-5-98

S.A. PCB, SG 5050 AMP BOARD

SIZE D | PROJECT NO. 96CD14 | PART NO. 30D25002 | REV. B

DO NOT SCALE DRAWING | SCALE 2=1 | SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	EO #3549	9-15-97	GI
	B	EO #3566	11-17-97	GI
	C	EO #		



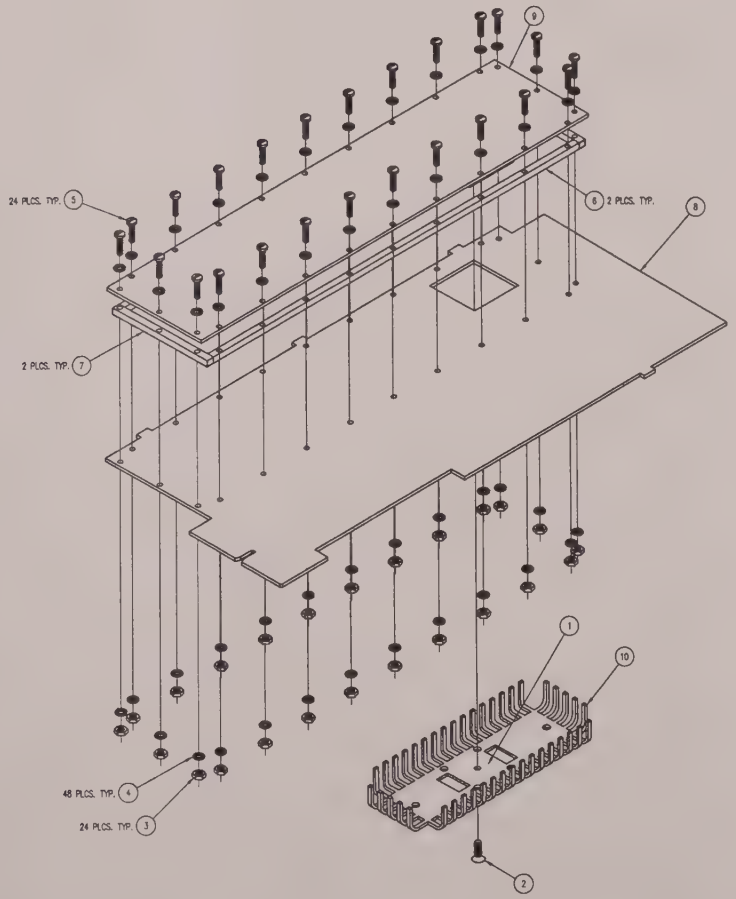
ITEM	QTY.	PART NO.	DESCRIPTION
5	1	30D23903	S.A. PCB, SG 5050 DDS BOARD
4	1	30D23702	S.A. PCB, SG 5050 VCO BOARD
3	6	22B29700	SPACER, BRASS ROUND, 4-40 X 1/4" X 1/2"
2	11	20SM21PP	SCREW, #4-40 X 1/4", PAN HEAD, PHILLIPS
1	11	20WA2000	WASHER, SS, #4, INTERNAL STAR

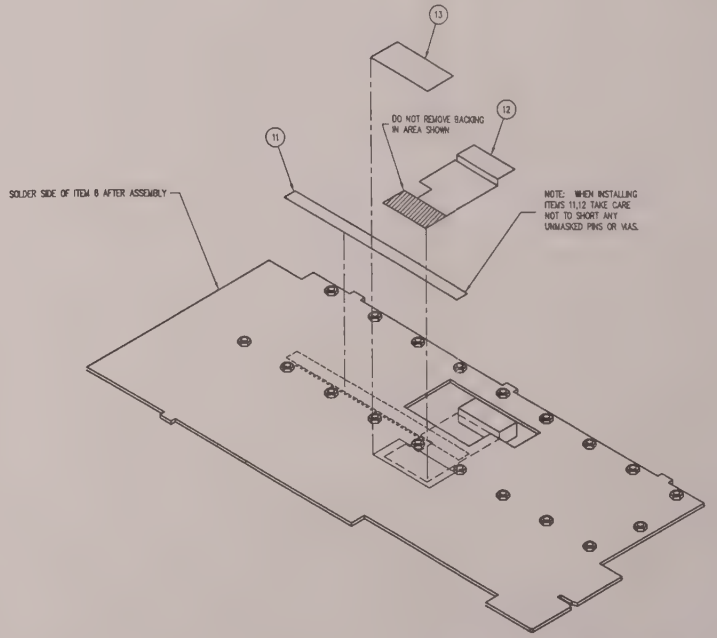
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ±1/64 .XX ± .010 ±0°30' .XXX ± .005

DO NOT SCALE DRAWING

DRAWN BY C.A.	DATE 7-10-97	S.A. SG 5050 DDS BOARD W/ VCO BOARD
CHECKED BY DDW	DATE 9-15-97	
APPROVED BY GI	DATE 9-15-97	MATERIAL / FINISH
REVISION C.A.	DATE 3-4-99	DRAWING SIZE / COLOR
SIZE C	PROJECT NO. 96E014	PART NO. 31C24700 REV. C
SCALE 1=1		SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ECO 63548	9-15-97	MLS
	B	ECO #		




13
DO NOT REMOVE BACKING IN AREA SHOWN
12
11
SOLDER SIDE OF ITEM 8 AFTER ASSEMBLY
NOTE: WHEN INSTALLING ITEMS 11,12 TAKE CARE NOT TO SHORT ANY UNMASKED PINS OR VIAS.

ITEM	QTY	PART NO.	DESCRIPTION
10	1	31B23700	S.A. HEATSINK MODIFIED R.F. AMPLIFIER
9	1	30D25002	S.A. PCB, SG 5050 OUTPUT AMP BOARD
8	1	30D24802	S.A. PCB, SG 5050 OUTPUT DECK BOARD
12	1	24802100	COPPER FOIL, 1" X 2.25"
11	1	24802000	COPPER FOIL, .25" X 4"
7	2	24801600	MOUNTING RAIL, SMALL, R.F. AMPLIFIER
6	2	24800300	MOUNTING RAIL, R.F. AMPLIFIER
13	A/R	22A11000	TAPE, INSULATING
5	24	20SM12PS	SCREW, #2-56 X 3/8", PAN HEAD, SLOTTED
4	48	20W11000	WASHER, #2, INTERNAL STAR
3	24	20KP1000	NUT, HEX, #2-56
2	1	21SA21FP	SCREW, SS, #4-40 X 1/4", FLAT HEAD, PHILLIPS
1	A/R	18A00100	THERMAL COMPOUND

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± 1/64 .XX ± .010 .XXX ± .005

DRAWN BY	C.A.	7-15-97
CHECKED BY	DOW	9-15-97
APPROVED BY	MLS	9-15-97
RELEASED	C.A.	9-29-98

S.A. SG 5050 OUTPUT DECK W/ OUTPUT AMP BOARD

SIZE D | PROJECT NO. 9REQ114 | PART NO. 31D28600 | REV. B

DO NOT SCALE DRAWING | SCALE 1=1 | SHEET 1 OF 1

REVISIONS				
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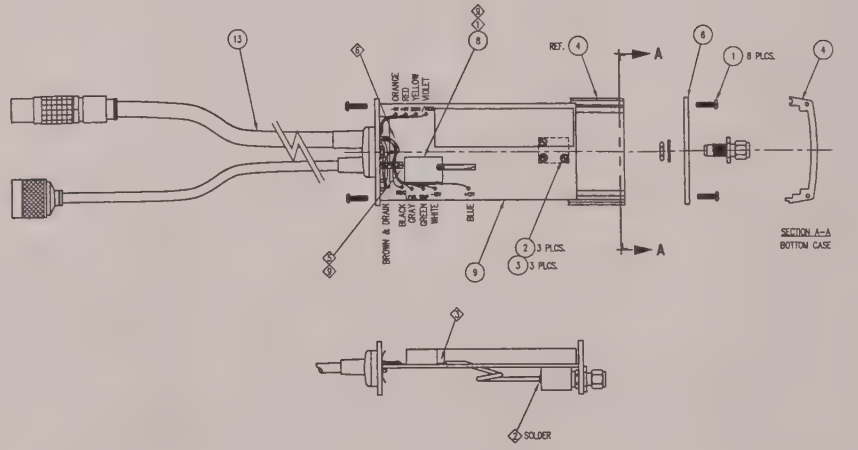
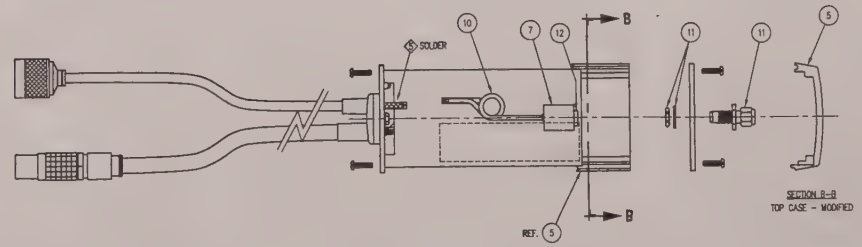
	B	ECO #		





NOTES:

1. ITEM (8) MUST BE MODIFIED TO CLEAR CABLES ITEMS (10) AND (13). (MUST SEAT FLUSH TO BOARD)
2. INSTALL ITEM (12) INTO ITEM (7), THEN INSTALL ITEM (10) AND SOLDER.
3. INSTALL ASSY OF NOTE 2 FROM BACK OF BOARD, WIRE END OF ITEM (10) MUST BE FLAT ON P.C. BOARD TRACE PRIOR TO SOLDERING.
4. ASSEMBLE ITEM (11) TO ITEM (8) AND THEN ASSEMBLE TO CASE ITEM (4). INSERT P.C. BOARD ASSY (9) AND THEN ALIGN & FASTEN ITEM 13 TO ASSY. CABLE END OF COAXIAL CABLE SHOULD MATE WITH P.C. BOARD. CENTER CONDUCTOR SHOULD BE FLAT ON P.C. BOARD. CARE SHOULD BE TAKEN TO TRIM ANY EXCESS STRANDS FROM [redacted]
5. SOLDER COAXIAL CABLE TO P.C. BOARD APPLYING A SOLDER BEAD ON EACH SIDE OF COAXIAL CABLE AND SOLDER CENTER CONDUCTOR.
6. ROUTE AND SOLDER COLOR CODED WIRES AS SHOWN.
7. INSTALL TOP HALF OF CASE AND 4 SCREWS. REMOVE BOTTOM HALF OF CASE AND SOLDER BOTH SIDES OF COAXIAL CABLE TO P.C. BOARD. SOLDER ITEM (8) IN PLACE.
8. INSTALL ITEM (8) AND TACK SHIELD IN PLACE.
9. ASSEMBLE ITEM (5) TO TOP OF CASE, REMOVE ITEM (4) FROM BACK, SOLDER ITEM (8) TO BACK SIDE, REFERENCE NOTE 5, SOLDER BACK SIDE OF COAXIAL CABLE, REASSEMBLE ITEM (4) TO BACK OF CASE.

ITEM	QTY	PART NO.	DESCRIPTION
12	1	45869200	CONNECTOR, SMA TO SEMI-RIGID
11	1	45869100	CONNECTOR, SMA TO SMA
10	1	32823900	S.A. OUTPUT CABLE, LEVELING HEAD
13	1	31C29400	CABLE/END PLATE ASSY
9	1	30C23501	S.A. PCB, SG 5050 LEVELING HEAD
8	1	24821200	SHIELD, CIRCUIT BOARD, 0.50" X 0.75" X 0.3"
7	1	24800800	CONNECTOR MOUNTING BLOCK, LEVELING HEAD
6	1	23C12200	COVER, END, FRONT LEVELING HEAD
5	1	23806600	LEVELING HEAD CASE, MODIFIED
4	1	23806400	LEVELING HEAD CASE
3	3	20W1000	WASHER, #2, INTERNAL STAR
2	3	20SA18PS	SCREW, SS, #2-56 X 1/8", PAN HEAD, SLOTTED
1	8	20SA12PS	SCREW, SS, #2-56 X 3/8", PAN HEAD, SLOTTED

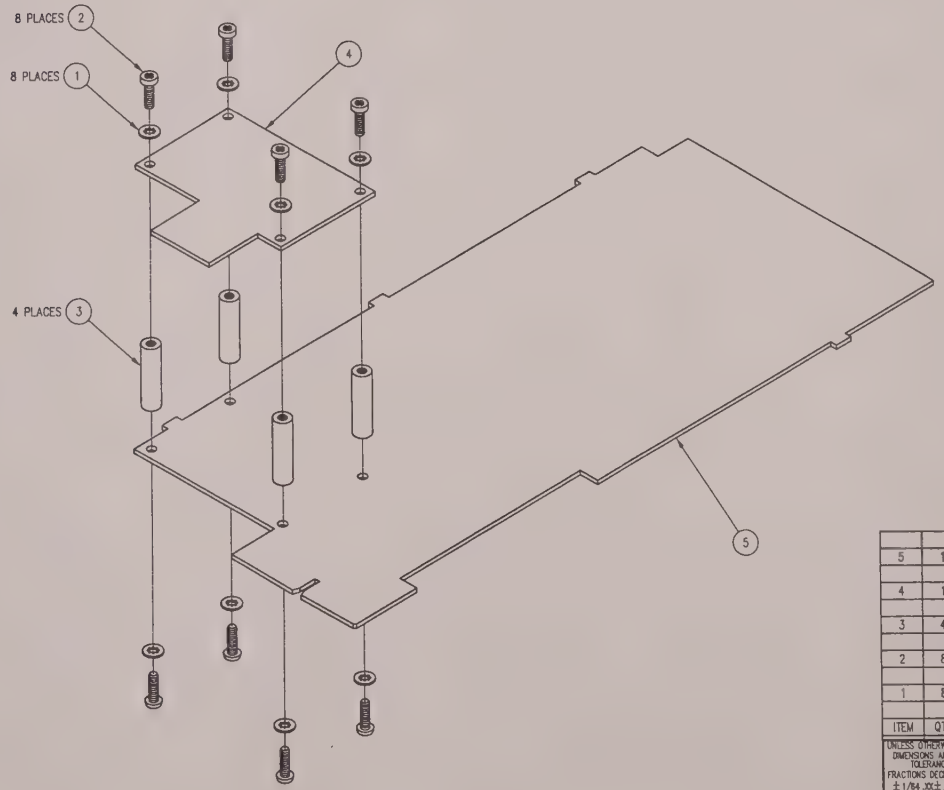
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS .XX DECIMALS ANGLES ± 1/64 .XX ± .010 .XXX ± .005

DRAWN BY C.A.	DATE 10-15-97	S.A. SG 5050 LEVELING HEAD
ENGINEER BY WWW	DATE 1-15-98	
APPROVED BY NI-S	DATE 1-15-98	MATERIAL
RELEASED CA	DATE 1-4-98	FINISH
		MANUFACTURER
		DATE

SIZE D | PRODUCT NO. 96ED14 | PART NO. 31D29300 | REV. B

DO NOT SCALE DRAWING | SCALE 1=1 | SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	EO #		



ITEM	QTY.	PART NO.	DESCRIPTION
5	1	30D23300	S.A. PCB, SG 5050 CPU BOARD
4	1	30D23200	S.A. PCB, SG 5050 GPIB BOARD
3	4	22A38200	SPACER, BRASS ROUND, 4-40 X 1/4" X 29/32"
2	8	20SW22PP	SCREW, #4-40 X 3/8", PAN HEAD, PHILLIPS
1	8	20WA2000	WASHER, SS, #4, INTERNAL STAR

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
±1/64 .XX± .010 ±0°30'
.XXX± .005

DRAWN BY C.A. DATE 2-20-97
CHECKED BY DATE
APPROVED BY DATE
REVISION DATE

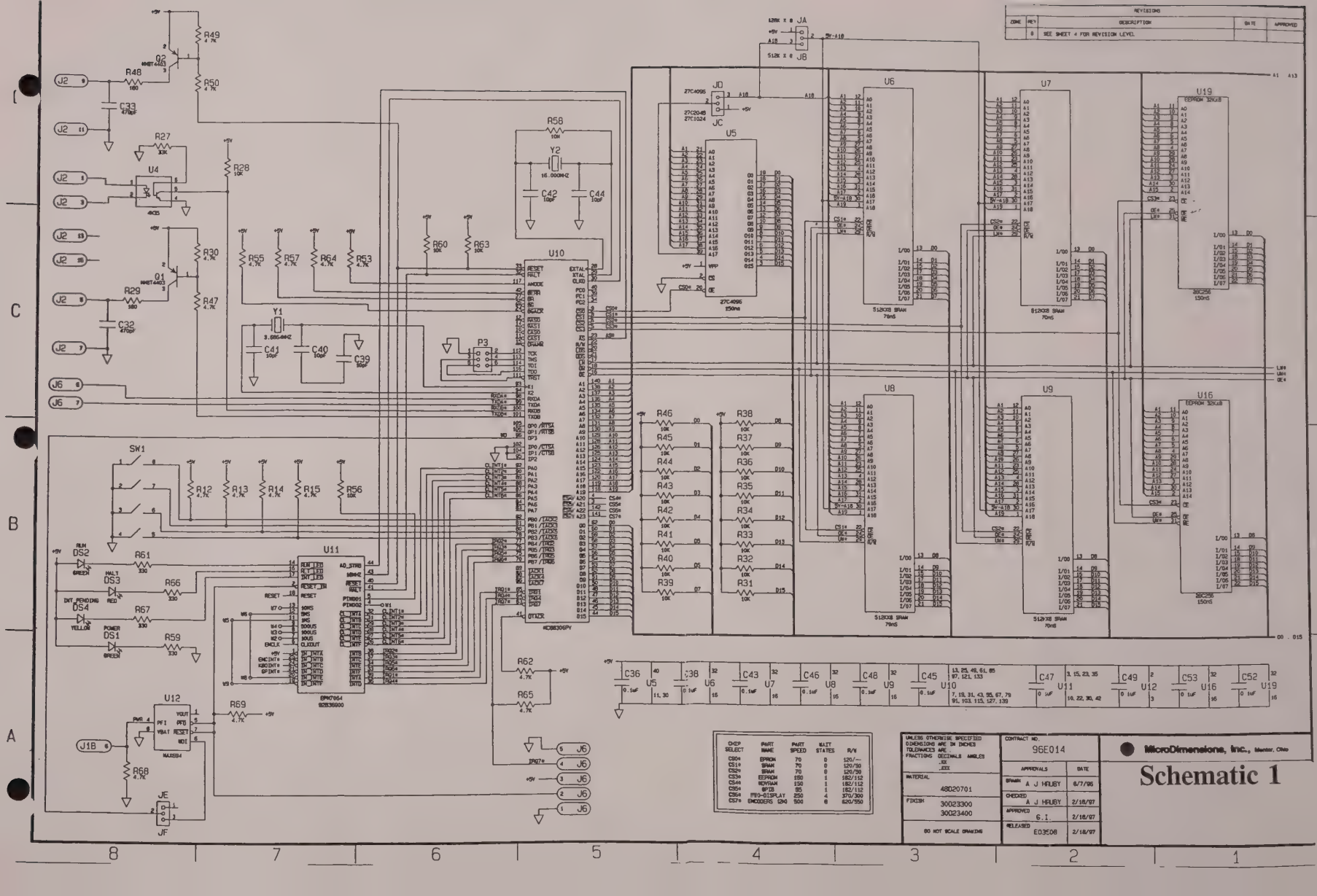
S.A. SG 5050 CPU BOARD
W/ GPIB BOARD

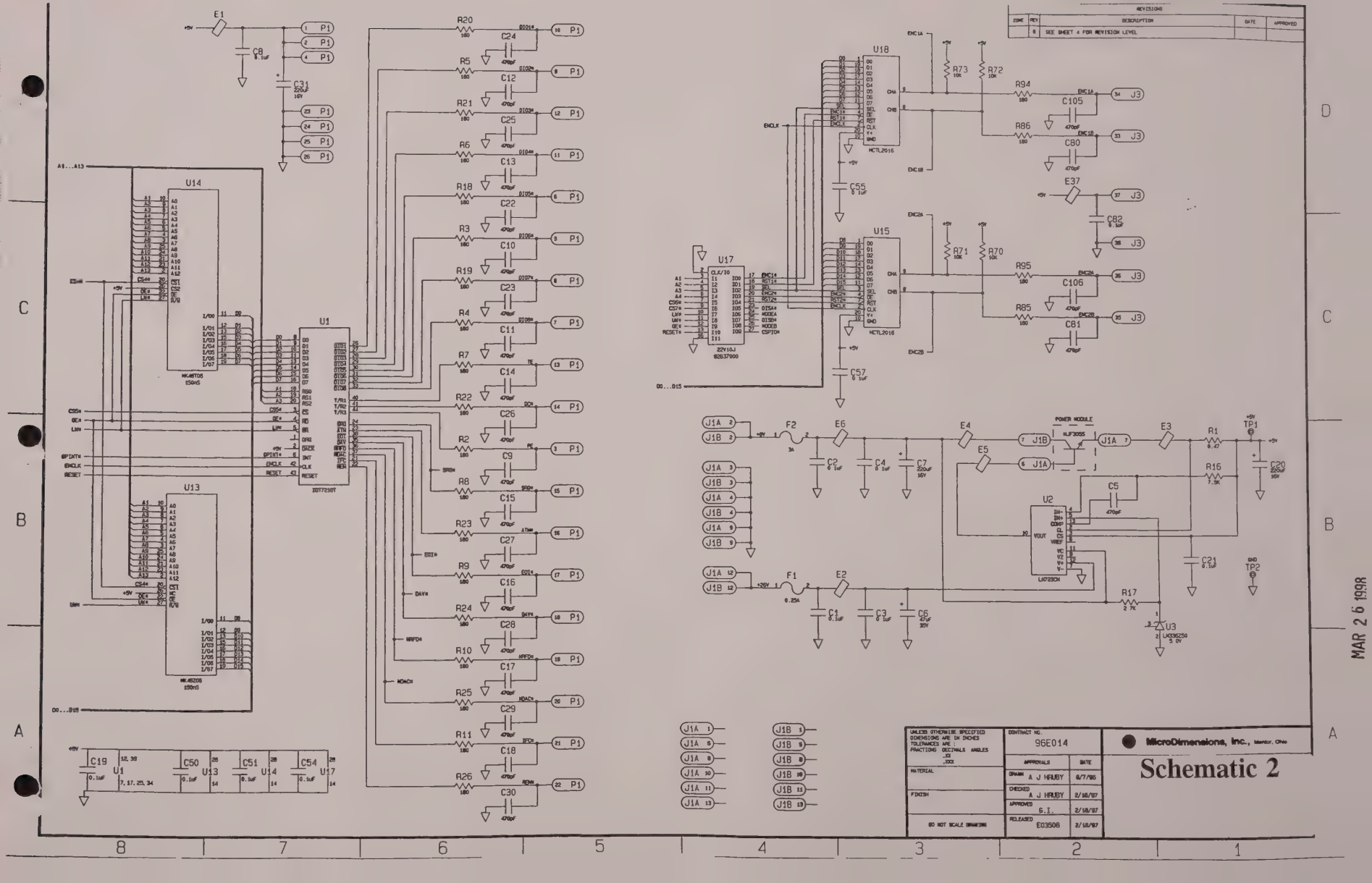
MATERIAL FINISH
SHRINKAGE COLOR

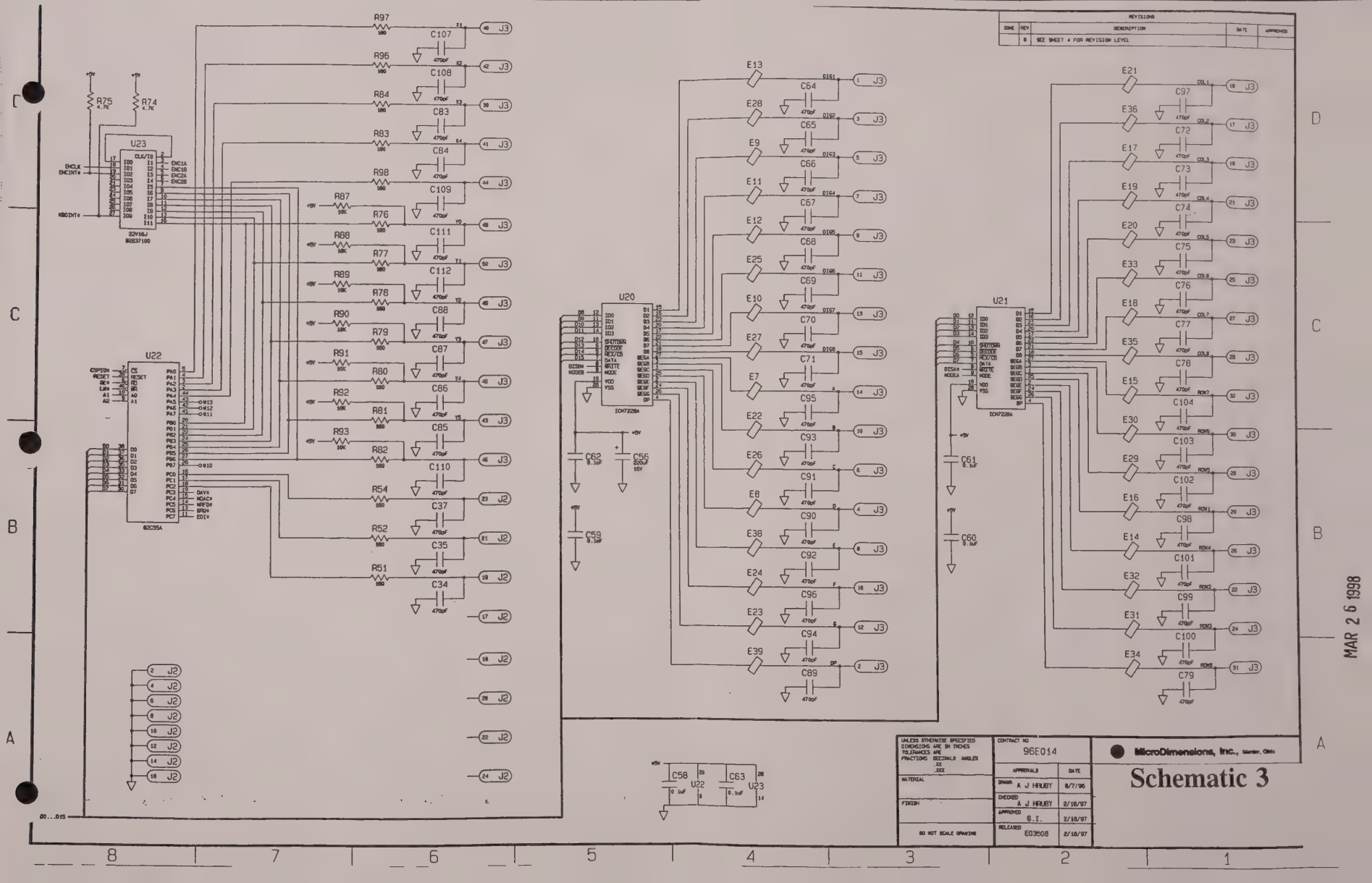
SIZE C | PROJECT NO. 96E014 | PART NO. 31C34800 | REV. A

DO NOT SCALE DRAWING | SCALE 1=1 | SHEET 1 OF 1

SECTION 9
DIAGRAMS, SCHEMATICS AND ILLUSTRATIONS


REVISIONS
ZONE REV DESCRIPTION DATE APPROVED
B SEE SHEET 4 FOR REVISION LEVEL.
U10
MC68306PV
U11
EPM7064
U5
U6
U7
U8
U9
U10
U11
U12
U16
U19
Y1
16.000MHz
Y2
SW1
P3
JA
JB
JC
JD
JE
JF
DS1
DS2
DS3
DS4
Q1
Q2
U4
MAX694
Schematic 1
MicroDimensions, Inc., Mentor, Ohio
CONTRACT NO. 96E014
MATERIAL 48020701
FINISH 30023300 30023400
DO NOT SCALE DRAWING
APPROVALS DATE
DRAWN A J HAUBY 6/7/96
CHECKED A J HAUBY 2/18/97
APPROVED G.L. 2/18/97
RELEASED E03508 2/18/97
MAR 26 1998


REVISIONS
ZONE | REV | DESCRIPTION | DATE | APPROVED
SEE SHEET 4 FOR REVISION LEVEL
U1
U13
U14
U15
U17
U18
U2
U3
IDT7210T
MCTL2016
LH0023CH
Schematic 2
MicroDimensions, Inc.,
96E014
E03508
MAR 26 1998


REVISIONS
ZONE REV DESCRIPTION DATE APPROVED
B SEE SHEET 4 FOR REVISION LEVEL
U23
U22
U20
U21
R75 4.7K
R74 4.7K
C107
C108
C83
C84
C109
C111
C112
C88
C87
C86
C85
C110
C37
C35
C34
C64
C65
C66
C67
C68
C69
C70
C71
C95
C93
C91
C90
C92
C96
C94
C89
C97
C72
C73
C74
C75
C76
C77
C78
C104
C103
C102
C98
C101
C99
C100
C79
C62 0.1uF
C56 220uF 16V
C59 0.1uF
C61 0.1uF
C60 0.1uF
C58 0 uF
C63 0.1uF
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX .XXX
MATERIAL
FINISH
DO NOT SCALE DRAWING
CONTRACT NO 96E014
APPROVALS DATE
DRAWN A J HANLEY 8/7/96
CHECKED A J HANLEY 2/18/97
APPROVED G.I. 2/18/97
RELEASED E03508 2/18/97
MicroDimensions, Inc., Manteca, CA
Schematic 3
MAR 26 1998

REVISIONS				
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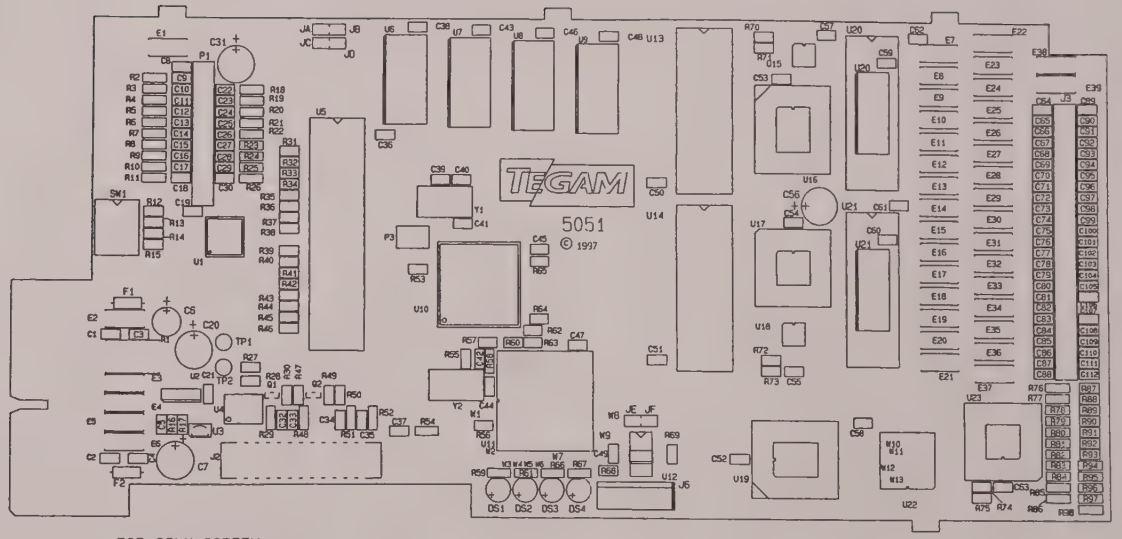


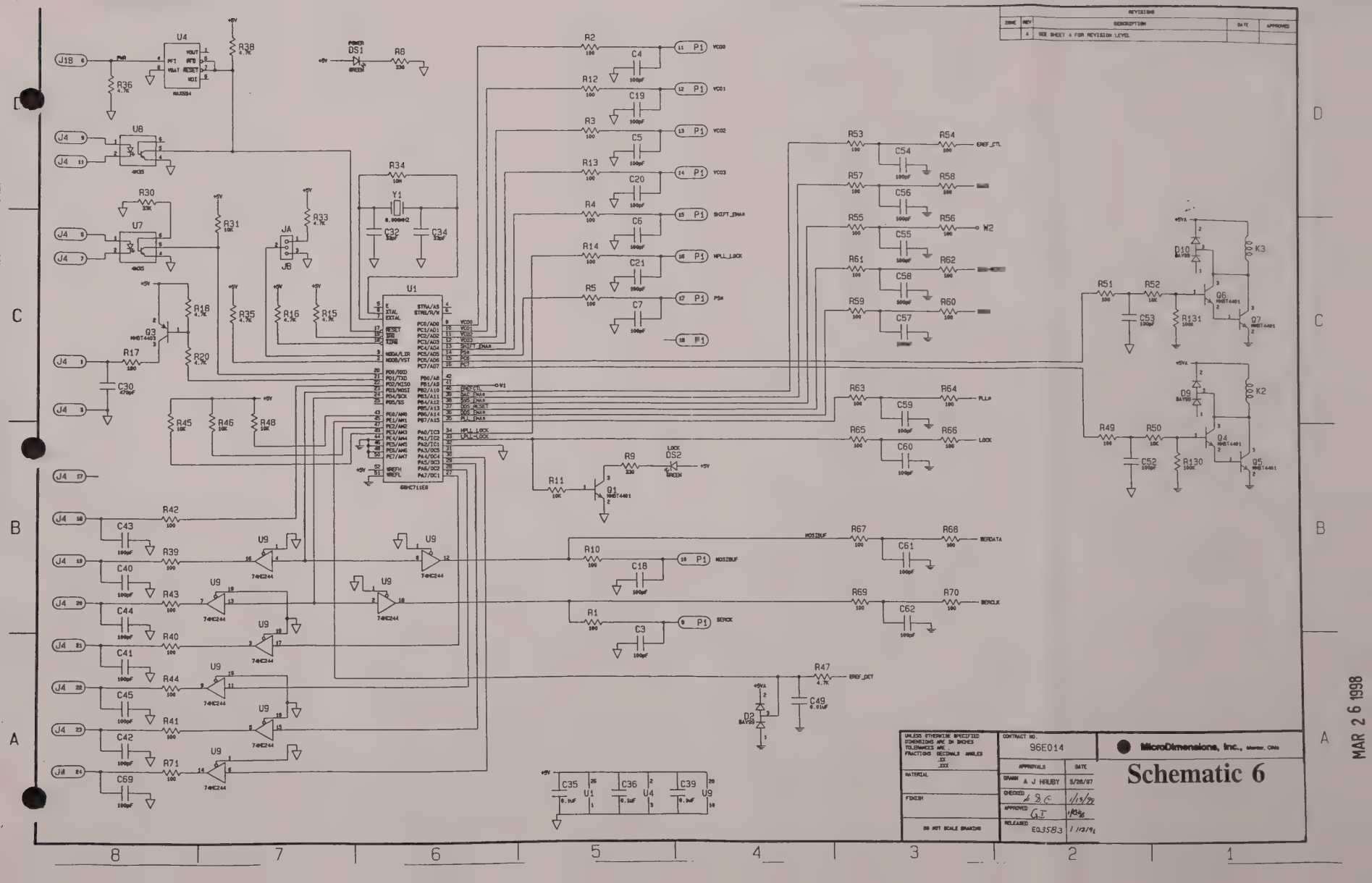
TOP SILK SCREEN

TEGAM P/N 389505100 MicroDimensions, Inc. 48D20701 2-14-97

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE : FRACTIONS DECIMALS ANGLES .XX .XXX	CONTRACT NO. 96E014	MicroDimensions, Inc., Manor, OHIO
	APPROVALS	DATE
MATERIAL	DRAWN A J HAUBY	8/7/95
FINISH	CHECKED A J HAUBY	2/18/97
	APPROVED G.I.	2/18/97
DO NOT SCALE DRAWING	RELEASED E03508	2/18/97

Schematic 4

MAR 2 6 1998


REVISIONS
ZONE
REV
DESCRIPTION
DATE
APPROVED
A
SEE SHEET 4 FOR REVISION LEVEL
U1
U4
U7
U8
U9
Y1
DS1
DS2
Q1
Q3
Q4
Q5
Q6
Q7
D2
D9
D10
K2
K3
JA
JB
R1
R2
R3
R4
R5
R9
R10
R11
R12
R13
R14
R34
R36
R38
R42
R43
R44
R45
R46
R47
R48
R53
R54
R57
R58
R59
R60
R61
R62
R63
R64
R65
R66
R67
R68
R69
R70
R71
C1
C3
C4
C5
C6
C7
C18
C19
C20
C21
C30
C32
C34
C35
C36
C39
C40
C41
C42
C43
C44
C45
C49
C54
C55
C56
C57
C58
C59
C60
C61
C62
C69
VCO0
VCO1
VCO2
VCO3
SHIFT_ENAB
PSA
MPLL_LOCK
PLL_LOCK
EREF_CTL
EREF_DET
W1
W2
MOSIBUF
SERDATA
SERCLK
LOCK
UNLOCK
UNLOCK_LOCK
UNLOCK_UNLOCK
UNLOCK_PLL
UNLOCK_SDS
UNLOCK_DAC
UNLOCK_RESET
UNLOCK_ENAB
UNLOCK_PSA
UNLOCK_SHIFT
UNLOCK_VCO
UNLOCK_PLL_LOCK
UNLOCK_MPLL_LOCK
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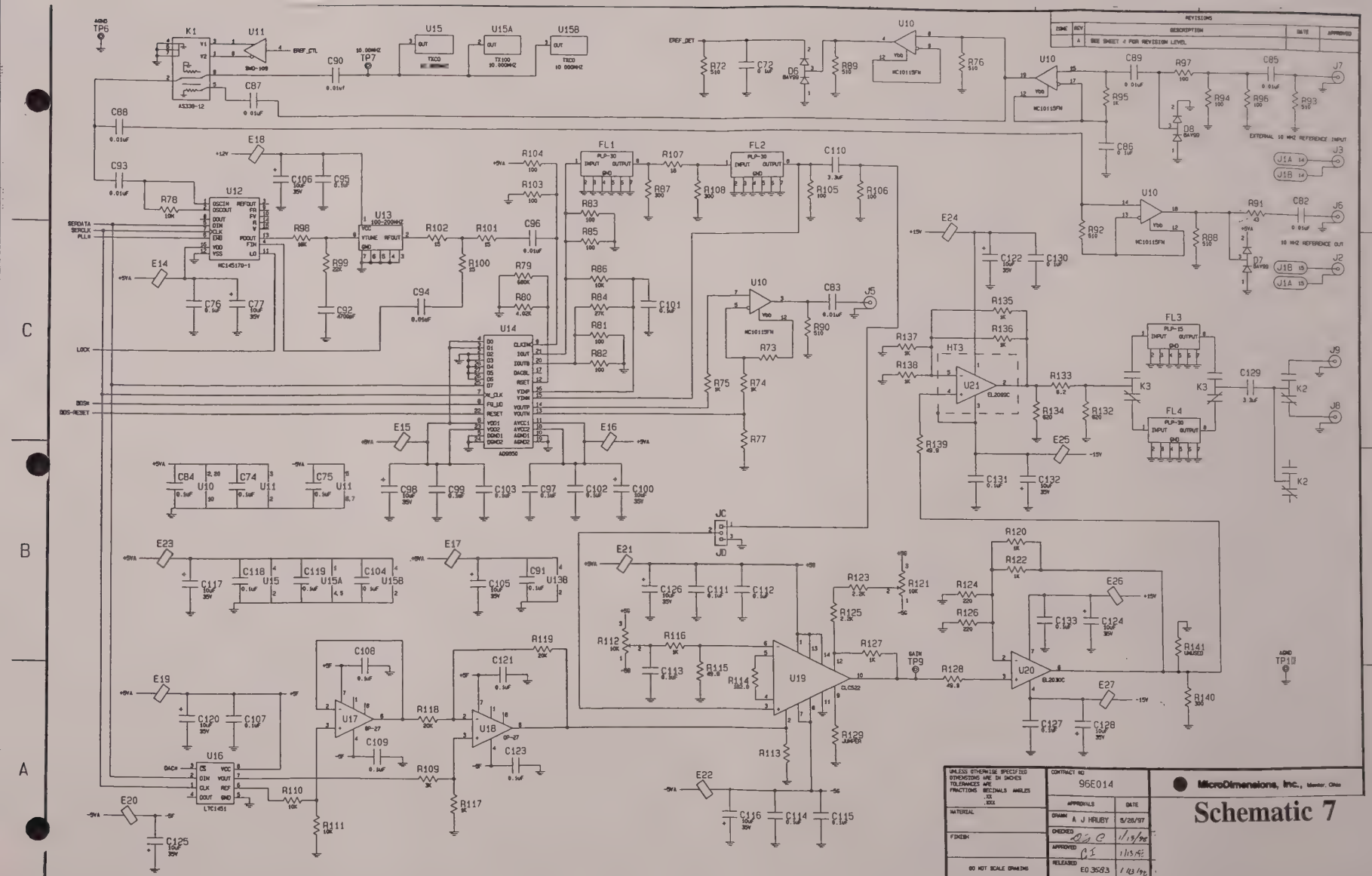
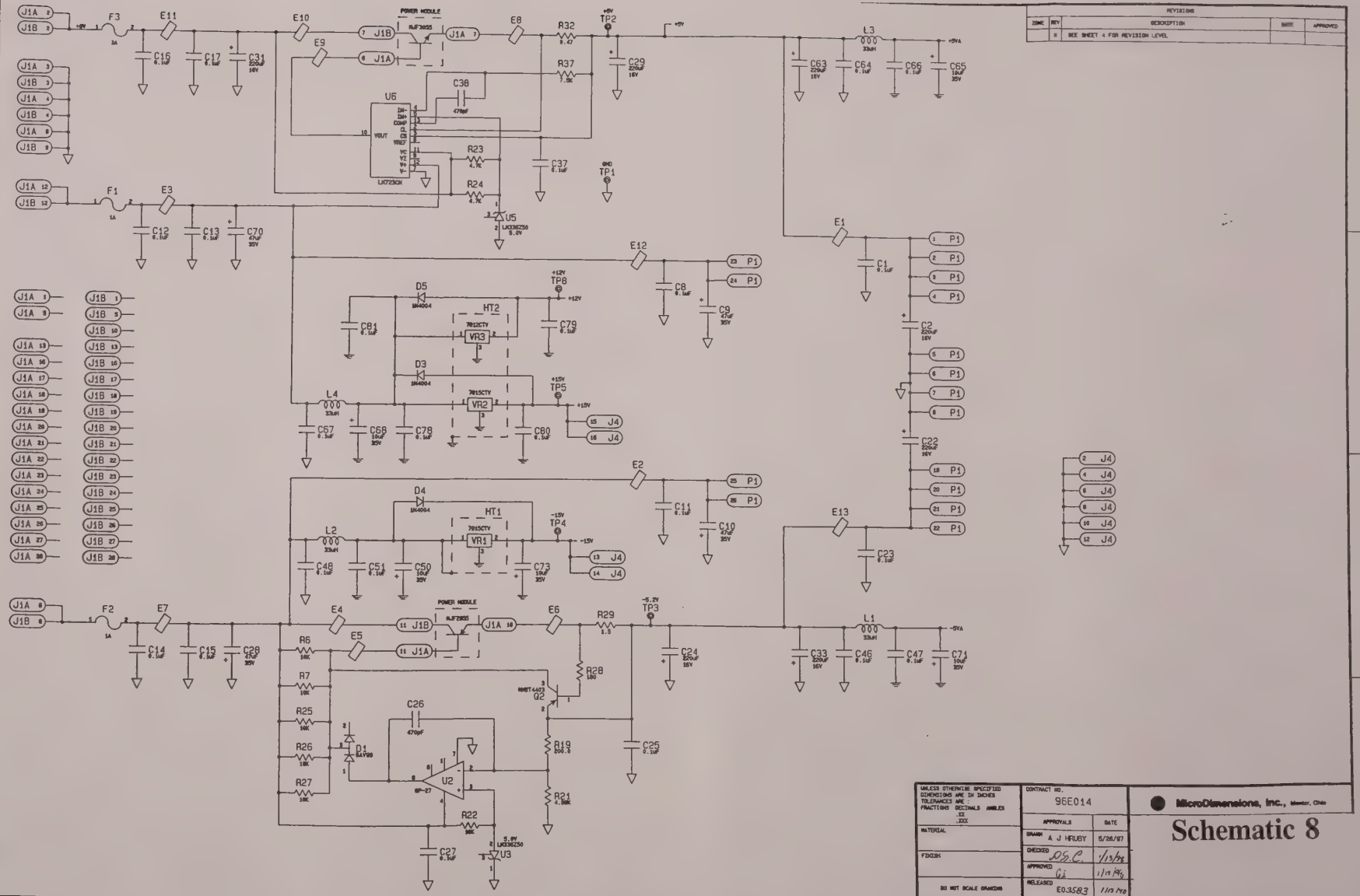
UNLOCK_SERDATA
UNLOCK_SERCL


REVISIONS
ZONE REV DESCRIPTION DATE APPROVED
A SEE SHEET 2 FOR REVISION LEVEL
Schematic 7
MicroDimensions, Inc., Manor, Ohio
CONTRACT NO 96E014
APPROVALS DATE
DRAWN A J HRUBY 5/28/97
CHECKED 1/15/98
APPROVED 1/13/98
RELEASED E0.3583 1/13/98
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS ±.XX .XXX ANGLES ±
MATERIAL
FINISH
DO NOT SCALE DRAWING
MAR 26 1998


REVISIONS
ZONE REV DESCRIPTION DATE APPROVED
B SEE SHEET 4 FOR REVISION LEVEL
F3 3A
F1 1A
F2 1A
POWER MODULE
MJF2955
MJF2905
U6
LX1723CH
U5 LX1336250 5.0V
U2 OP-27
U3 LX1336250 5.0V
D5 1N4004
D3 1N4004
D4 1N4004
D1 1N4148
HT2 7912CTV VR3
HT1 7915CTV VR1
7915CTV VR2
Q2 MMBT4403
L4 33uH
L2 33uH
L3 33uH
L1 33uH
E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
E11
E12
E13
TP1 GND
TP2 +5V
TP3 -5.2V
TP4 -15V
TP5 +15V
TP8 +12V
+5VA
-5VA
P1
J4
MATERIAL
FINISH
DO NOT SCALE DRAWING
CONTRACT NO. 96E014
APPROVALS DATE
DRAWN A J HRUBY 5/28/97
CHECKED 1/13/98
APPROVED 1/13/98
RELEASED E03583 1/13/98
MicroDimensions, Inc., Mentor, Ohio
Schematic 8
MAR 26 1998

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
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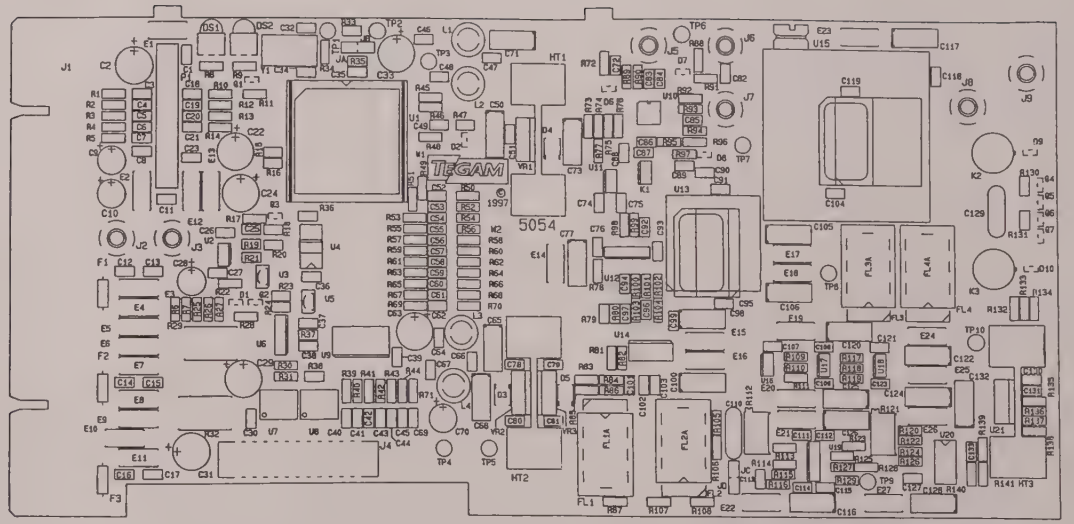
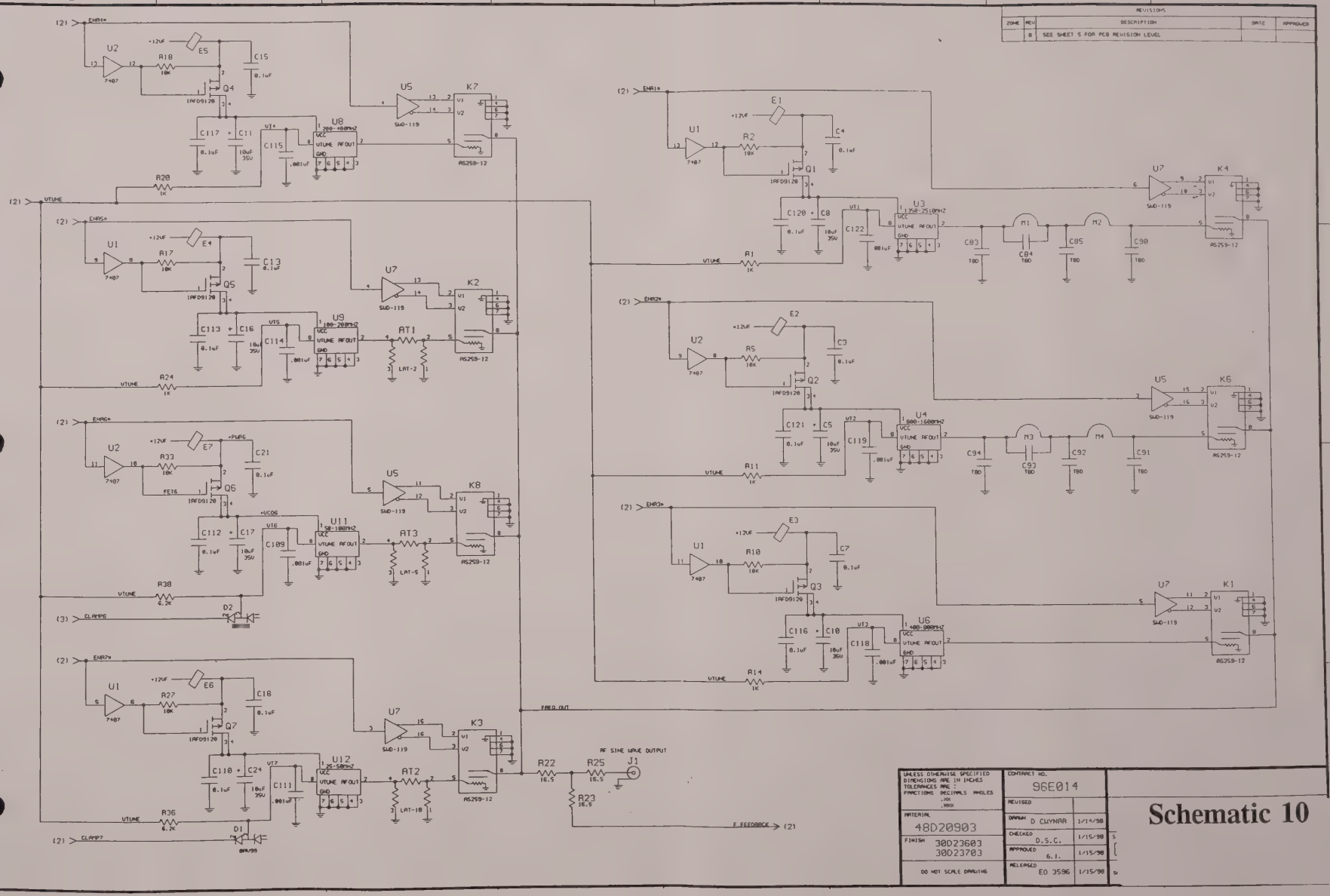


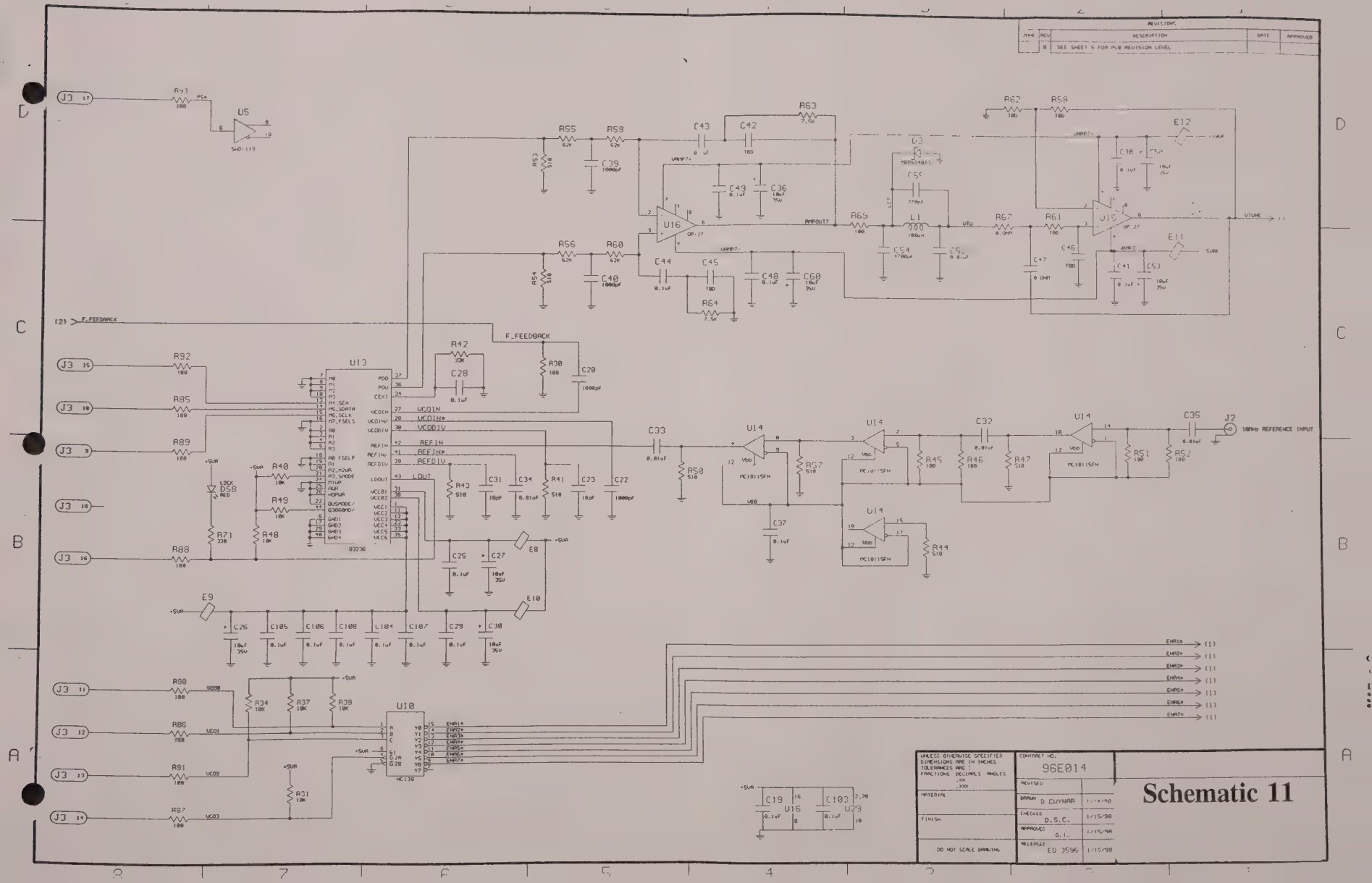
SILK SCREEN MicroDimensions, Inc. 48D20803 5-30-97

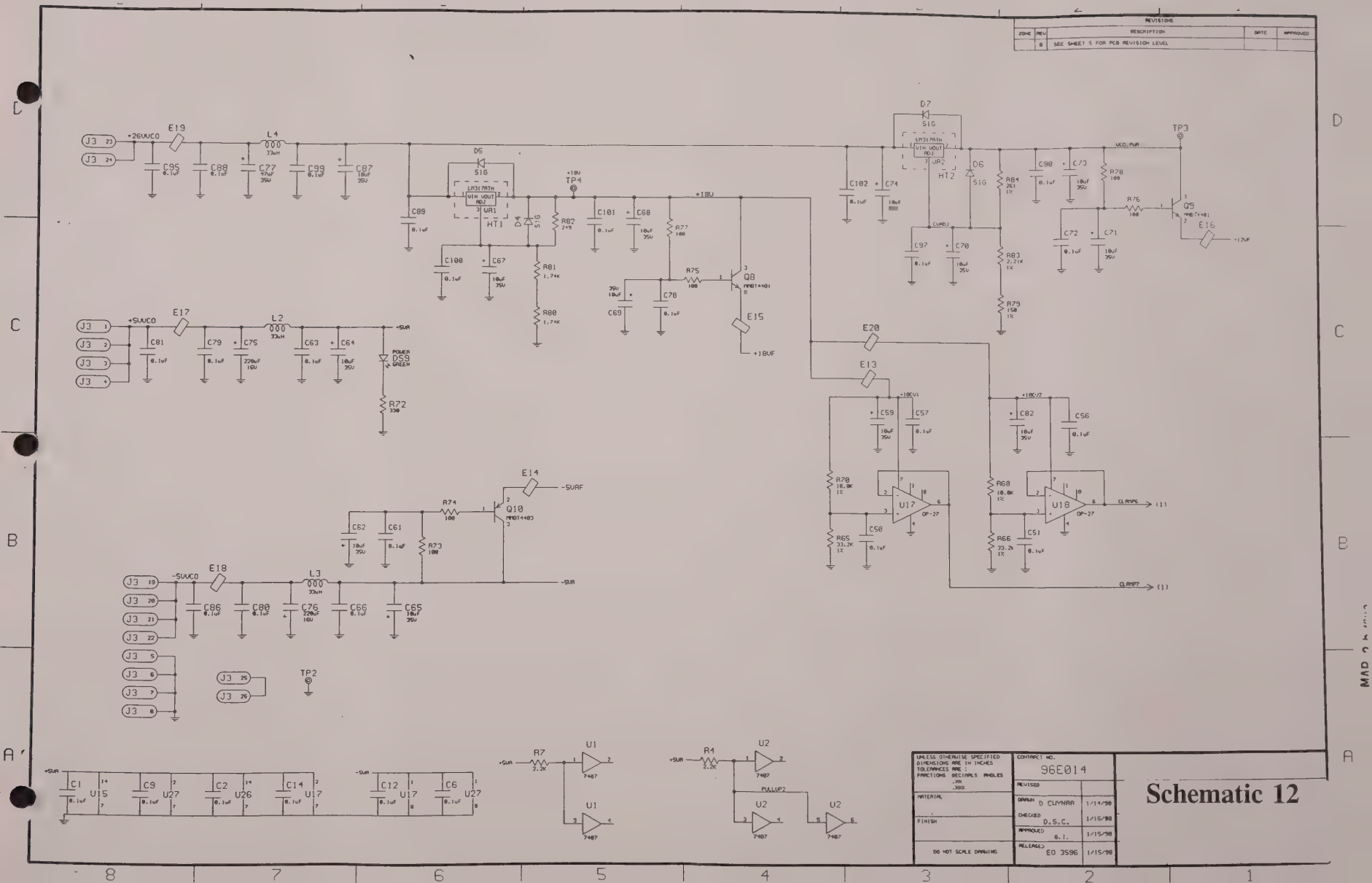
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE : FRACTIONS DECIMALS ANGLES .XX .XXX	CONTRACT NO. 96E014	MicroDimensions, Inc., Manor, Ohio
MATERIAL	APPROVALS	DATE
FINISH	DRAWN A J HRUBY	5/28/9
DO NOT SCALE DRAWING	CHECKED	1/13/9
	APPROVED	1/13/9
	RELEASED EO #3583.	1/13/9

Schematic 9

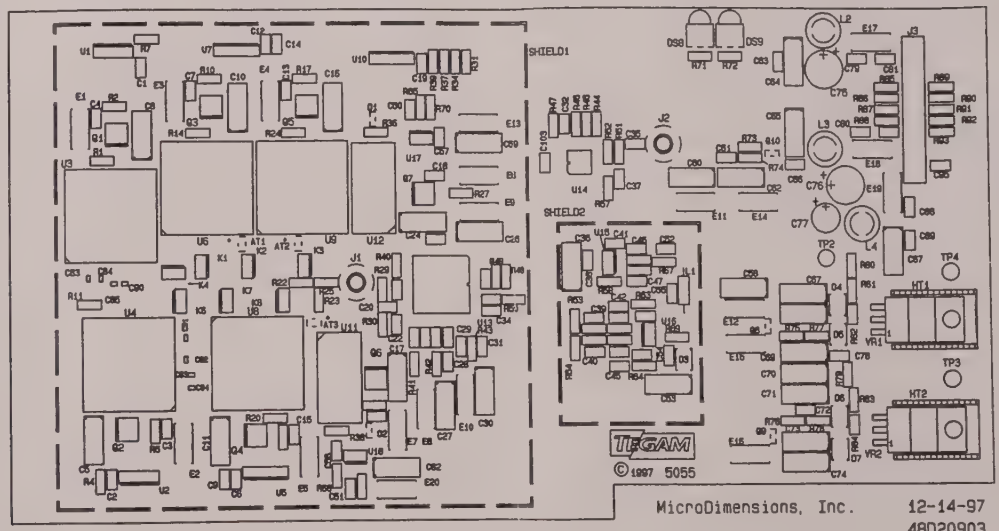
MAR 2 6 1998


REVISIONS
ZONE REV DESCRIPTION DATE APPROVED
B SEE SHEET 5 FOR PCB REVISION LEVEL
ENA1a
ENA2a
ENA3a
ENA4a
VTUNE
CLAMPS
CLAMP7
FREQ OUT
RF SINE WAVE OUTPUT
F FEEDBACK
U1
U2
U3
U4
U5
U7
U8
U9
U11
U12
K1
K2
K3
K4
K5
K6
K7
K8
Q1
Q2
Q3
Q4
Q5
Q6
Q7
D1
D2
J1
AT1
AT2
AT3
M1
M2
M3
M4
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX
MATERIAL 48D20903
FINISH 30D23603 30D23703
DO NOT SCALE DRAWING
CONTRACT NO. 96E014
REVISED
DRAWN D CLYMER 1/14/98
CHECKED D.S.C. 1/15/98
APPROVED G.I. 1/15/98
RELEASED EO 3596 1/15/98
Schematic 10


REVISIONS
ZONE | REV | DESCRIPTION | DATE | APPROVED
B | SEE SHEET 5 FOR PLB REVISION LEVEL
F_FEEDBACK
U5
U16
OP-27
U15
OP-27
U13
Q2236
U14
MC10115FN
U10
HC138
E12
E11
E8
E9
E10
J2
10MHz REFERENCE INPUT
VTUNE
LOCK
DS8
LED
U16
C19
C103
U29
CONTRACT NO.
96E014
REVISED
DRAWN D. CLYNAR 1/14/98
CHECKED D.S.C. 1/15/98
APPROVED G.I. 1/15/98
RELEASED EO 3596 1/15/98
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±
MATERIAL
FINISH
DO NOT SCALE DRAWING
Schematic 11


REVISIONS
ZONE REV DESCRIPTION DATE APPROVED
B SEE SHEET 5 FOR PCB REVISION LEVEL
+26VUCO
E19
L4
33uH
C95 0.1uF
C88 0.1uF
C77 470uF 35V
C99 0.1uF
C87 10uF 35V
D5
SIG
LM317ATH
VIN VOUT ADJ
VR1
HT1
+18U
TP4
C89 0.1uF
C100 0.1uF
C67 10uF 35V
R82 249
R81 1.74K
R80 1.74K
C101 0.1uF
C68 10uF 35V
R77 100
R75 100
Q8
MRF1440
C69 10uF 35V
C78 0.1uF
E15
+18UF
E20
D7
SIG
LM317ATH
VIN VOUT ADJ
VR2
HT2
D6
SIG
C102 0.1uF
C74 10uF
R84 261 1%
R83 2.21K 1%
R79 150 1%
C97 0.1uF
C70 10uF 35V
(VADJ)
VCO_PWR
TP3
C90 0.1uF
C73 10uF 35V
R78 100
R76 100
Q9
MRF1440
C72 0.1uF
C71 10uF 35V
E16
+12UF
+5VUCO
E17
L2
33uH
J3 1
J3 2
J3 3
J3 4
C81 0.1uF
C79 0.1uF
C75 220uF 16V
C63 0.1uF
C64 10uF 35V
+5UR
POWER
DS9
GREEN
R72 330
E13
+18CV1
C59 10uF 35V
C57 0.1uF
R70 10.0K 1%
R65 33.2K 1%
C58 0.1uF
U17
OP-27
+18CV2
C82 10uF 35V
C56 0.1uF
R68 10.0K 1%
R66 33.2K 1%
C51 0.1uF
U18
OP-27
CLAMPS
(1)
CLAMP7
(1)
E14
-5VAF
R74 100
Q10
MRF1440
C62 10uF 35V
C61 0.1uF
R73 100
-5UR
-5VUCO
E18
L3
33uH
J3 19
J3 20
J3 21
J3 22
J3 5
J3 6
J3 7
J3 8
C86 0.1uF
C80 0.1uF
C76 220uF 16V
C66 0.1uF
C65 10uF 35V
J3 25
J3 26
TP2
+5UR
C1 0.1uF
U15
C9 0.1uF
U27
C2 0.1uF
U26
C14 0.1uF
U17
-5UR
C12 0.1uF
U17
C6 0.1uF
U27
+5UR
R7 2.2K
U1
7407
U1
7407
+5UR
R4 2.2K
U2
7407
PULLUP
U2
7407
U2
7407
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE :
FRACTIONS DECIMALS ANGLES
.XX
.XXX
MATERIAL
FINISH
DO NOT SCALE DRAWING
CONTRACT NO.
96E014
REVISED
DRAWN D CLYMAR 1/14/98
CHECKED D.S.C. 1/15/98
APPROVED G.I. 1/15/98
RELEASED EO 3596 1/15/98
Schematic 12
MAD 2 K

ZONE	REV	DESCRIPTION	DATE	APPROVED
	B	SEE SHEET 6 FOR PCB REVISION LEVEL		



MicroDimensions, Inc. 12-14-97
48D20903

TOP SILK SCREEN

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX	CONTRACT NO. 96E014		
MATERIAL	REVISED		ASSEMBLY, TOP SIDE SG 5050 VCO BOARD
FINISH	DRAWN D CRYMAR	1/14/98	
DO NOT SCALE DRAWING	CHECKED Q.S.C.	1/15/98	SIZE D CAGE SHEET NO. DWG. NO. 90D27202
	APPROVED S.I.	1/15/98	
	RELEASED EO 3598	1/15/98	SCALE NTS SHEET 4 OF 5

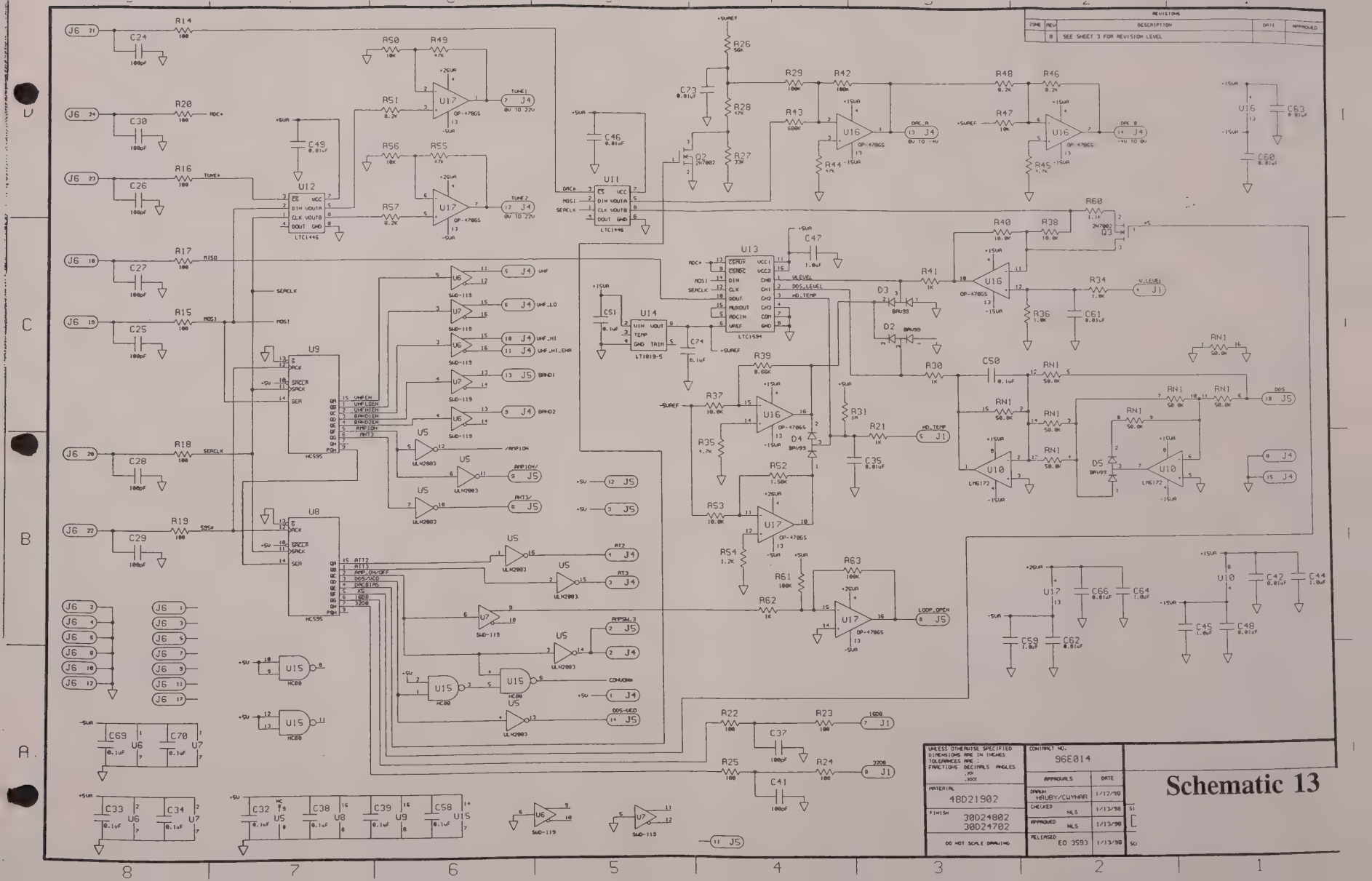
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	E.O. 49288	1/15/98	G.I.
	B	E.O. #		

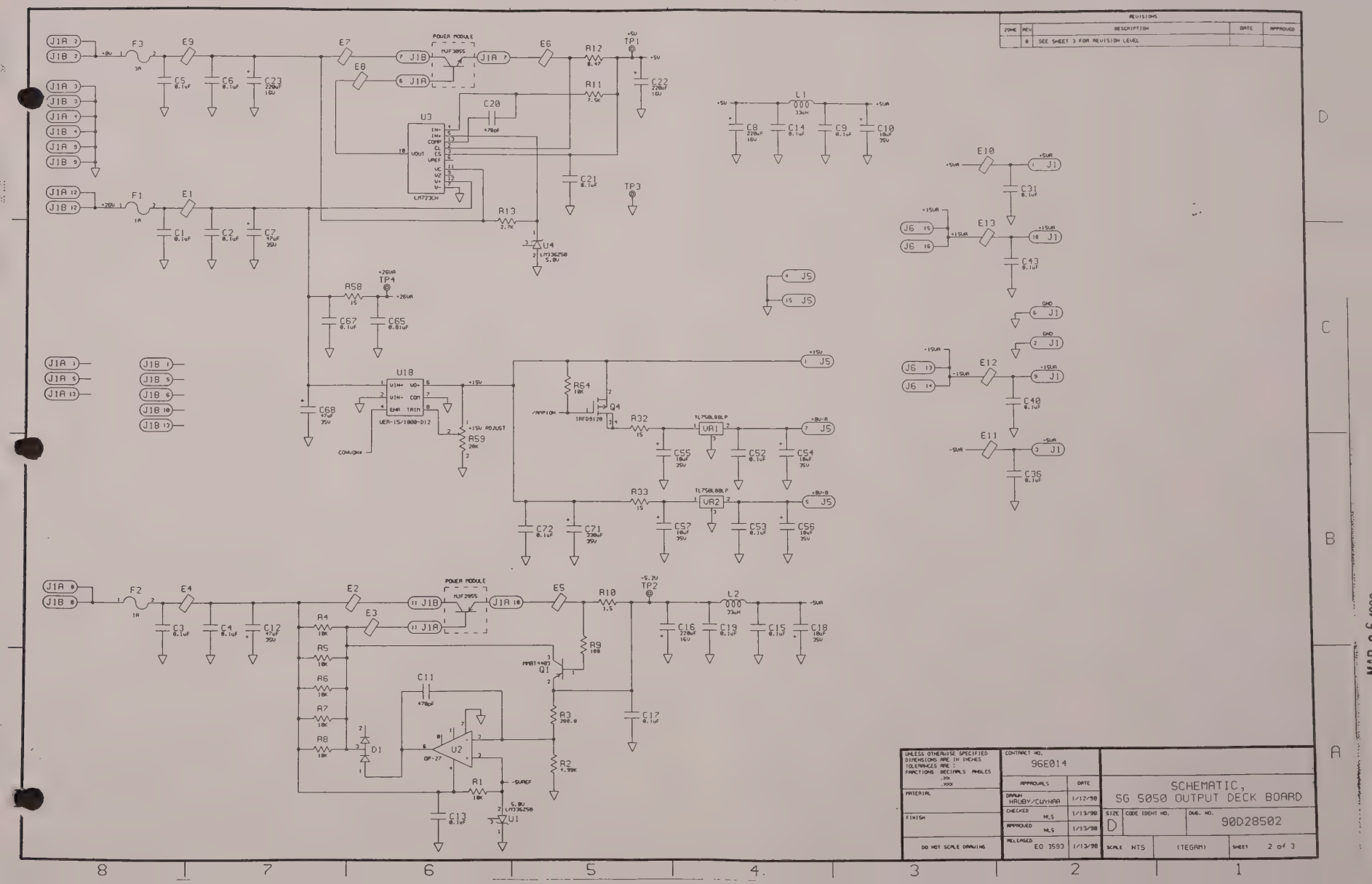
12-14-97 MicroDimensions, Inc.
4BD20903 BOTTOM SILK SCREEN

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX	CONTRACT NO. 96E014		
MATERIAL	REVISED		ASSEMBLY, BOTTOM SIDE SG 5050 VCO BOARD
FINISH	DRAWN D CHYNAR	1/14/98	
DO NOT SCALE DRAWING	CHECKED D.S.C.	1/15/98	SIZE D / CAGE IDENT NO. / DWG. NO. 90D27202
	APPROVED G.I.	1/15/98	
	RELEASED ED 3595	1/15/98	SCALE NTS / SHEET 5 OF 5

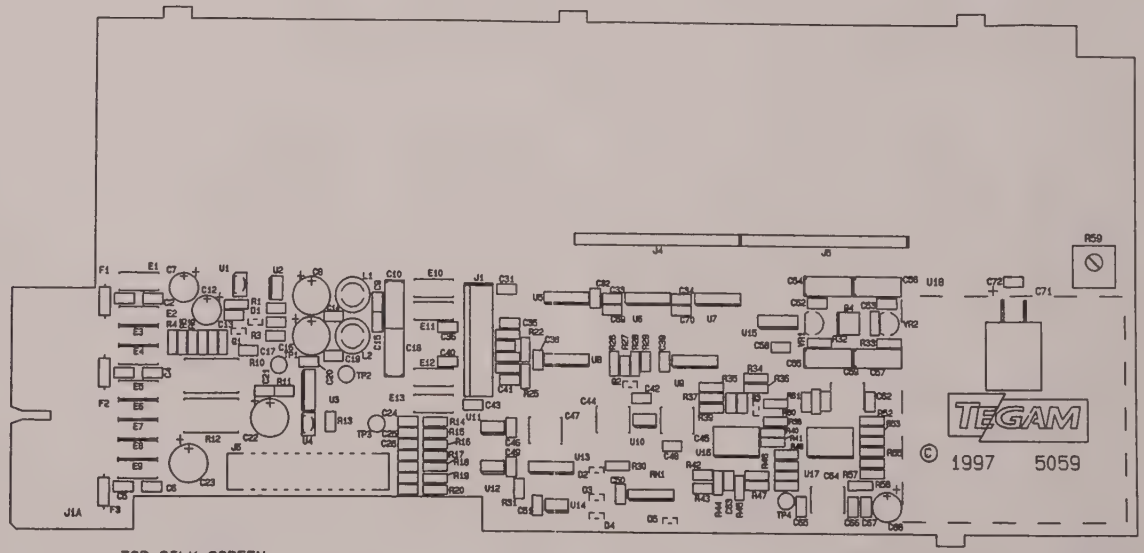
8 7 6 5 4 3 2 1

D C B A


REVISIONS
ZONE REV DESCRIPTION DATE APPROVED
B SEE SHEET 1 FOR REVISION LEVEL
Schematic 13
CONTRACT NO. 96E014
APPROVALS DATE
DRAWN HRUBY/CLWYMAN 1/12/98
CHECKED MLS 1/13/98
APPROVED MLS 1/13/98
RELEASED EO 3593 1/13/98
MATERIAL 48D21902
FINISH 30D24802 30D24702
DO NOT SCALE DRAWING
SIZE C
SCALE
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ±.XXX
+5VREF
-5VREF
+5VA
-5VA
+5V
-5V
+15VA
-15VA
+26VA
SEARCLK
MOSI
MISO
SERCLK
TUNE1
TUNE2
TUNE+
ADC+
595#
U1 U2 U3 U4 U5 U6 U7 U8 U9 U10 U11 U12 U13 U14 U15 U16 U17
R14 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 R31 R34 R35 R36 R37 R38 R39 R40 R41 R42 R43 R44 R45 R46 R47 R48 R49 R50 R51 R52 R53 R54 R55 R56 R57 R60 R61 R62 R63
C24 C25 C26 C27 C28 C29 C30 C33 C34 C35 C36 C37 C38 C39 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C51 C58 C59 C60 C61 C62 C63 C64 C65 C66 C69 C70 C74
RN1
D2 D3 D4 D5
Q2 Q3
J1 J2 J3 J4 J5 J6
DAC_A DAC_B
LOOP_OPEN
HD_TEMP
V_LEVEL
DDS
AMP_ON/OFF
/AMPION
AMPION/
ANT2
ANT3
BAND1
BAND2
UHF
UHF_LO
UHF_HI
UHF_HI_ENA
COM/ANN
DDS-VCO
1GDB
32DB
LTC1446
LTC1394
LT1019-5
MC595
MC88
ULN2003
SMD-119
OP-470GS
LM172
BAV99


REVISIONS
ZONE REV DESCRIPTION DATE APPROVED
B SEE SHEET 3 FOR REVISION LEVEL
POWER MODULE
MJF2955
LM723CH
LM336Z50
UEA-15/1000-D12
IRFD9120
IL750L80LP
MMBT4403
DP-27
+5V
+26VA
-26V
+15V
-15V
+8V-A
+8V-B
-5.2V
-5VA
+5VA
+15VA
-15VA
GND
+15V ADJUST
/ENABLE
COMM/ON#
SCHEMATIC,
SG 5050 OUTPUT DECK BOARD
CONTRACT NO. 96E014
DRAWN HALEY/CUYNAR 1/12/98
CHECKED M.S 1/13/98
APPROVED M.S 1/13/98
RELEASED EO 3593 1/13/98
SIZE D
CODE IDENT NO.
DWG. NO. 90D28502
SCALE NTS
(TEGAM)
SHEET 2 of 3
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE : FRACTIONS DECIMALS ANGLES .XX .XXX
MATERIAL
FINISH
DO NOT SCALE DRAWING

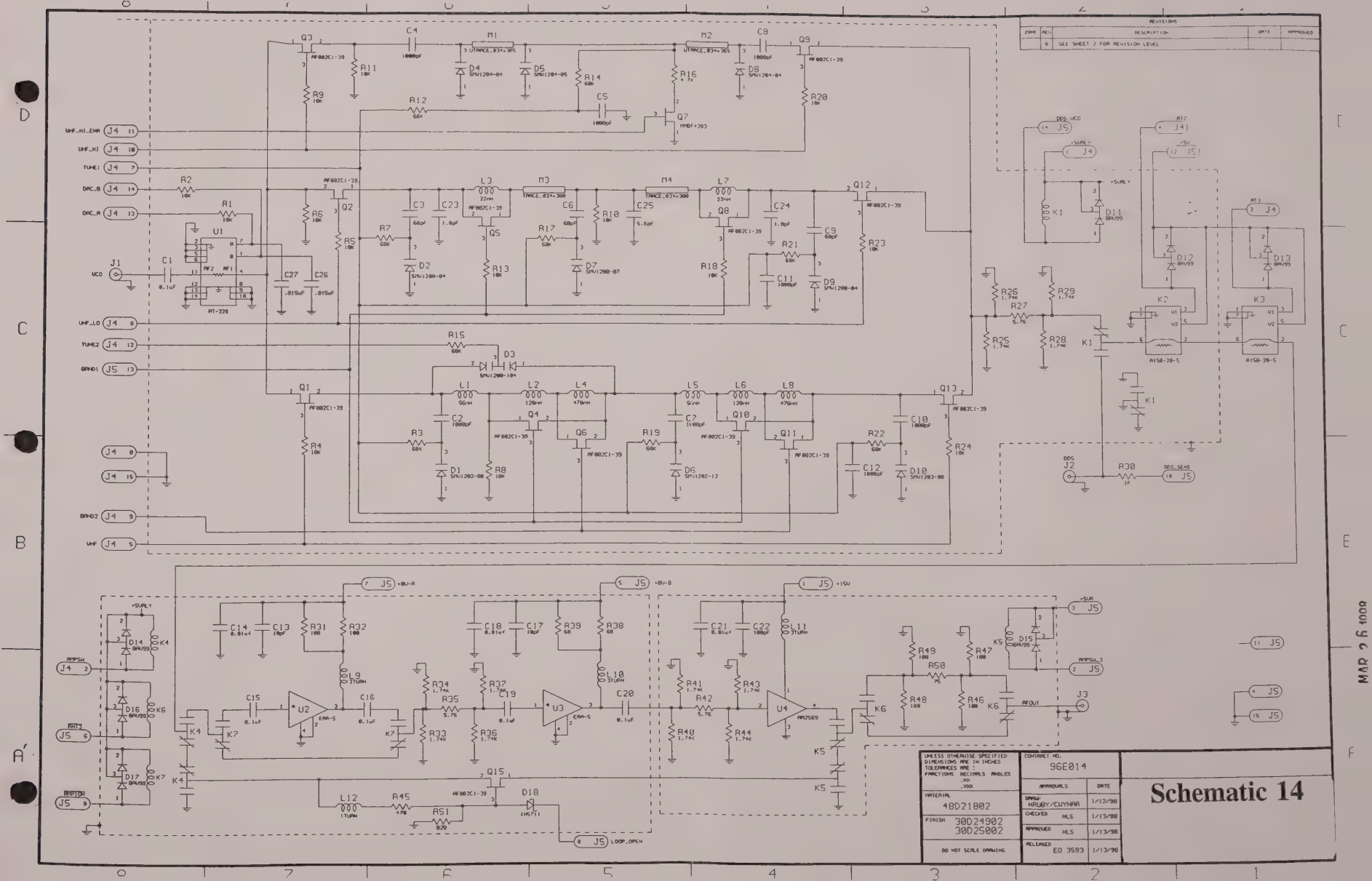
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	E.O.6383	1/13/98	MLS
	B	E.O.6		



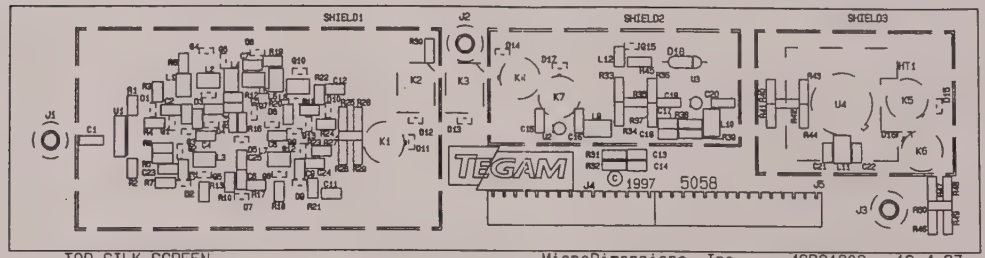
TOP SILK SCREEN
MicroDimensions, Inc. 48D21902 12-8-97

MAR 2 6 1998

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE : FRACTIONS DECIMALS ANGLES .XX .XXX	CONTRACT NO. 96E014		
MATERIAL	APPROVALS	DATE	SCHEMATIC, SG 5050 OUTPUT DECK BOARD
FINISH	DRAWN HRUBY/CHYNAR	1/12/98	
DO NOT SCALE DRAWING	CHECKED MLS	1/13/98	SIZE D CODE IDENT NO. DWG. NO. 90D28502
	APPROVED MLS	1/13/98	
	RELEASED ED 3923	1/13/98	SCALE NTS (TEGAM) SHEET 3 of 3


REVISIONS
ZONE REV DESCRIPTION DATE APPROVED
B SEE SHEET 2 FOR REVISION LEVEL
Q3 AF002C1-39
C4 1000pF
M1 UTRACE_.03+.305
M2 UTRACE_.03+.305
C8 1000pF
Q9 AF002C1-39
R11 10K
R9 10K
D4 SMV1204-04
D5 SMV1204-05
R14 68K
R16 1.7K
D8 SMV1204-04
R20 10K
R12 68K
C5 1000pF
Q7 MMBF4393
UHF_HI_ENA J4 11
UHF_HI J4 10
TUNE1 J4 7
DAC_B J4 14
DAC_A J4 13
R2 10K
R1 10K
R6 10K
Q2 AF002C1-39
R5 10K
U1
J1 VCO
C1 0.1uF
C27 .01uF
C26 .01uF
AT-339
C3 68pF
C23 1.8pF
L3 22nH
M3 TRACE_.03+.300
C6 68pF
C25 5.6pF
M4 TRACE_.03+.300
L7 22nH
Q12 AF002C1-39
C24 1.8pF
C9 68pF
R23 10K
Q5 AF002C1-39
R7 68K
R17 68K
R10 10K
Q8 AF002C1-39
R21 68K
R13 10K
D2 SMV1200-04
D7 SMV1200-07
R18 10K
C11 1000pF
D9 SMV1200-04
UHF_LO J4 6
TUNE2 J4 12
BAND1 J5 13
R15 68K
D3 SMV1200-104
L1 56nH
L2 120nH
L4 470nH
L5 56nH
L6 120nH
L8 470nH
Q13 AF002C1-39
Q1 AF002C1-39
C2 1000pF
C7 1400pF
C10 1000pF
R4 10K
Q4 AF002C1-39
Q6 AF002C1-39
Q10 AF002C1-39
Q11 AF002C1-39
R3 68K
R19 68K
R22 68K
R24 10K
D1 SMV1202-08
R8 10K
D6 SMV1202-12
C12 1000pF
D10 SMV1202-08
J4 8
J4 15
BAND2 J4 9
UHF J4 5
DDS VCO J5 1
+5VSW1 J4 1
+5V J5 12
A17 J4 4
A18 J4 3
K1
D11 BAV99
D12 BAV99
D13 BAV99
K2
K3
A150-20-5
R26 1.74K
R27 5.7K
R29 1.74K
R25 1.74K
R28 1.74K
DDS J2
R30 1K
DDS_SENS J5 18
+5VSW
+5V-A
+5V-B
+5V
AMPSW J4 2
ANT1 J5 6
ROTOR J5 8
D14 BAV99
D16 BAV99
D17 BAV99
K4
K6
K7
C14 0.01uF
C13 100pF
R31 100
R32 100
L9 3TURN
C15 0.1uF
U2 ERA-5
C16 0.1uF
R34 1.74K
R35 5.7K
R33 1.74K
C18 0.01uF
C17 100pF
R39 68
R38 68
L10 3TURN
C19 0.1uF
U3 ERA-5
C20 0.1uF
R37 1.74K
R36 1.74K
C21 0.01uF
C22 100pF
L11 3TURN
R41 1.74K
R42 5.7K
R43 1.74K
R40 1.74K
R44 1.74K
U4 AA2589
K5
D15 BAV99
R49 100
R50 PS
R47 100
R48 100
R46 100
AMPSW J5 3
RFOUT
J3
11 J5
4 J5
15 J5
Q15
L12 11TURN
R45 47Ω
R51 820
D18 1N5711
8 J5 LOOP_OPEN
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE : FRACTIONS DECIMALS ANGLES .XX± .XXX±
MATERIAL 48D21802
FINISH 30D24902 30D25002
DO NOT SCALE DRAWING
CONTRACT NO. 96E014
APPROVALS DATE
DRAW: HAUBY/CLYMAR 1/12/98
CHECKED MLS 1/13/98
APPROVED MLS 1/13/98
RELEASED EO 3593 1/13/98
Schematic 14
MAR 2 6 1999

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	E. O. #3593	1/13/98	MLS
	B	E. O. #		

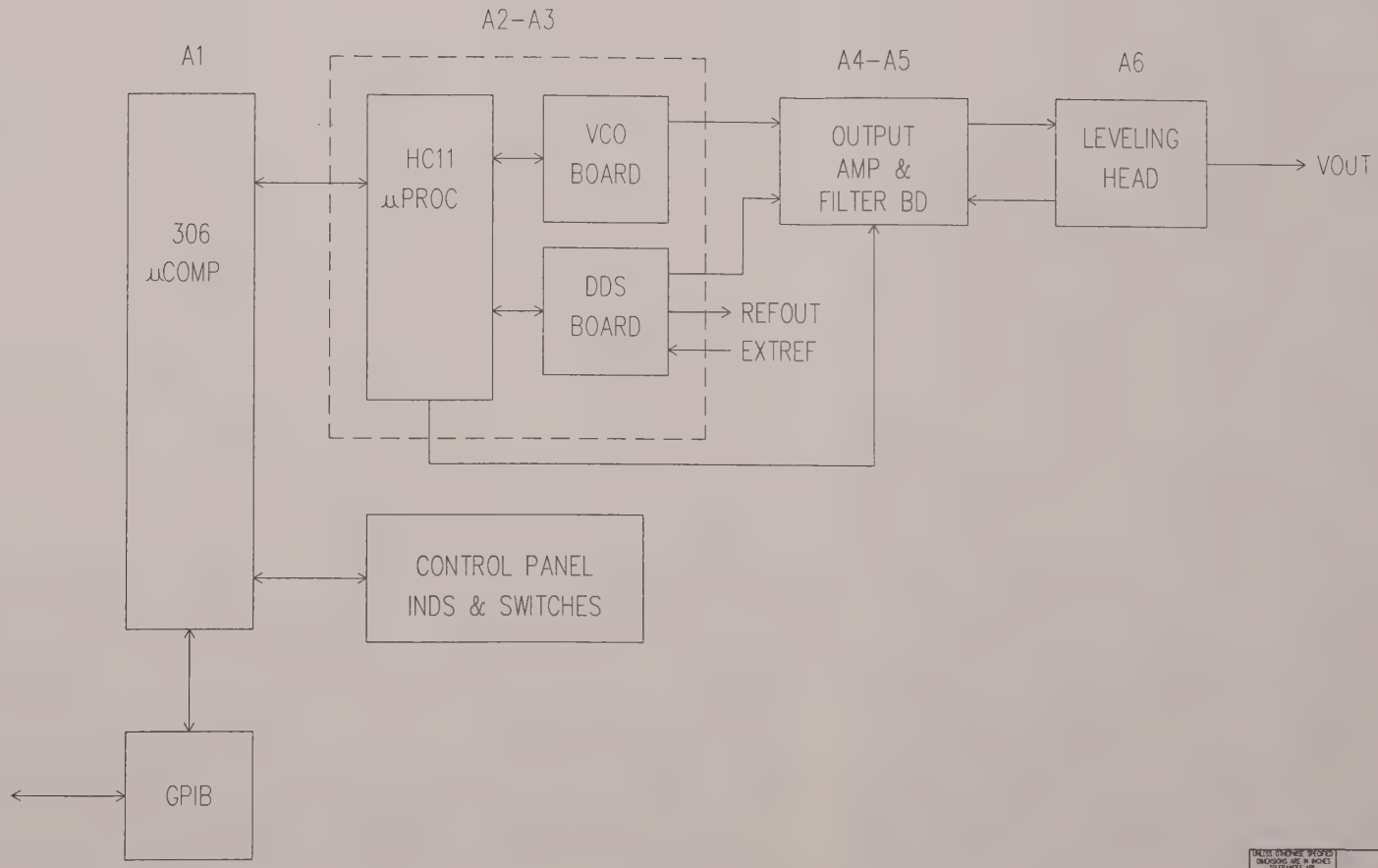


TOP SILK SCREEN

MicroDimensions, Inc. 48D21802 12-4-97

MAR 2 6 1998

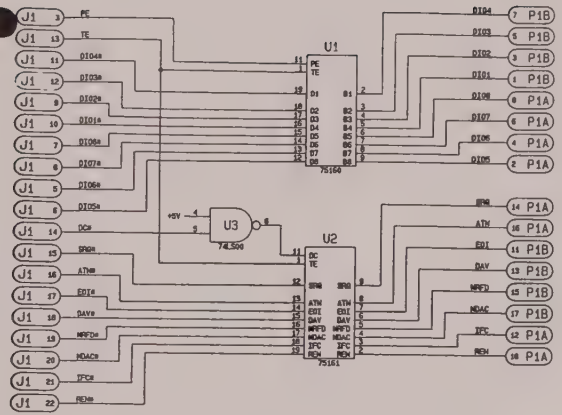
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE : FRACTIONS DECIMALS ANGLES .XX .XXX	CONTRACT NO. 96E014		
MATERIAL	APPROVALS	DATE	SCHEMATIC, SG 5050 OUTPUT AMP BOARD
FINISH	DRAWN HRUBY/CWYNAR	1/12/98	
	CHECKED MLS	1/13/98	SIZE D — CODE IDENT NO. — DWG. NO. 90D28602
DO NOT SCALE DRAWING	APPROVED MLS	1/13/98	
	RELEASED EO 3593	1/13/98	SCALE NTS — (TEGAM) — SHEET 2 of 2

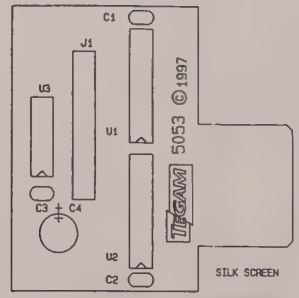


REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	EO 15423	5-14-96	Q
	B	EO # - REDRAWN		

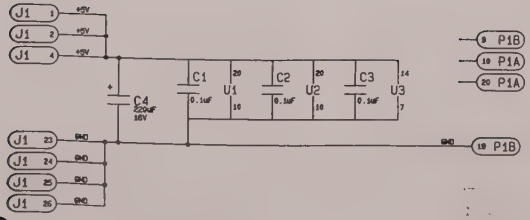
DRAWN BY	A.H	5/28/96	BLOCK DIAGRAM SG 5050
ENGINEER BY	A.H	6-14-96	
APPROVED BY	Q	6-14-96	
MFG/QA	QA	1-27-98	
SIZE	D	PROJECT NO 96E014	PART NO 93D03300 REV B
DO NOT SCALE DRAWING		SCALE 1=1	SHEET 1 OF 1

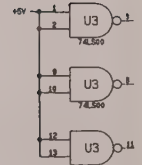
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	E0#3518	GI	3/17/97





TEGAM P/N 389505300
MicroDimensions, Inc. 4BC20601 2-18-97

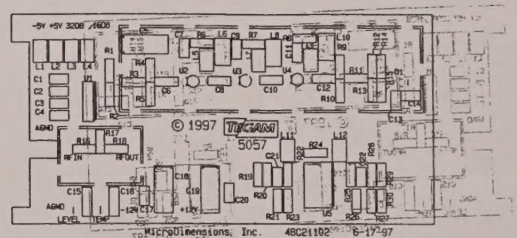




UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX	CONTRACT NO. 96E014	MicroDimensions, Inc., Manteca, CA	
MATERIAL	APPROVALS	DATE	SCHEMATIC, SG 5050 GPIB BOARD
FINISH	DRAWN A J HARVEY	6/26/96	
DO NOT SCALE DRAWING	CHECKED	3/13/97	SIZE D / CODE IDENT NO. / DWG. NO 90D26800
	APPROVED GI	3/17/97	
	RELEASED E03518	3/13/97	SCALE NTS / (TEGAM) / SHEET 1 of 1

MAR 26 1998

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	E.C.O. 3572	1/14/98	NLS



MicroDimensions, Inc. 48C21102 6-17-97
TOP SILK SCREEN

RFIN
RFOUT
U1
AK00202-24
160B
320B
L1 5.6uH
L2 5.6uH
L3 5.6uH
L4 5.6uH
-5V
160B
320B
C1 0.01uF
C2 0.01uF
C3 0.01uF
C4 0.01uF
R1 1.7K
R2 1.7K
R3 5.76
R4 1.7K
R5 1.7K
R6 24
R7 24
R8 24
R9 1.7K
R10 1.7K
R11 5.76
R12 1.7K
R13 1.7K
R14 NA
R15 NA
R16 14.0
R17 39.2
R18 10.0
C5 10uF 35V
C6 0.1uF
C7 0.01uF
C8 0.1uF
C9 0.01uF
C10 0.1uF
C11 0.01uF
C12 0.1uF
C13 0.01uF
C14 0.01uF
C15 10uF 16V
C16 10uF 16V
C17 0.01uF
C18 10uF 35V
C19 10uF 35V
C20 0.01uF
C21 0.01uF
C22 0.01uF
L5 3TURN
L6 6.8uH
L7 3TURN
L8 6.8uH
L9 3TURN
L10 6.8uH
L11 5.6uH
L12 5.6uH
D1 SMS3931-10
D1 SMS3931-10
U2 ERA-1
U3 ERA-1
U4 ERA-1
U5 OP-470GS
R19 10K
R20 1K
R21 1K
R22 68
R23 200K
R24 10K
R25 68
R26 82K
R27 1K
R28 1K
R29 10K
R30 82K
+12V
-12V
AGND
AGND1
TEMP
LEVEL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE : FRACTIONS DECIMALS ANGLES .XX .XXX	CONTRACT NO. 96E014	MicroDimensions, Inc., Marion, Ohio	
MATERIAL 48C21102	APPROVALS	DATE	Schematic 15
FINISH 30C23501	DRAWN MRUBY/CKYNAR	11/25/96	
DO NOT SCALE DRAWING	CHECKED DSC	4/4/13	
	APPROVED NLS	1/8/98	
	RELEASED ED-3872	12/2/97	